17059 USB6

USB Hub Training

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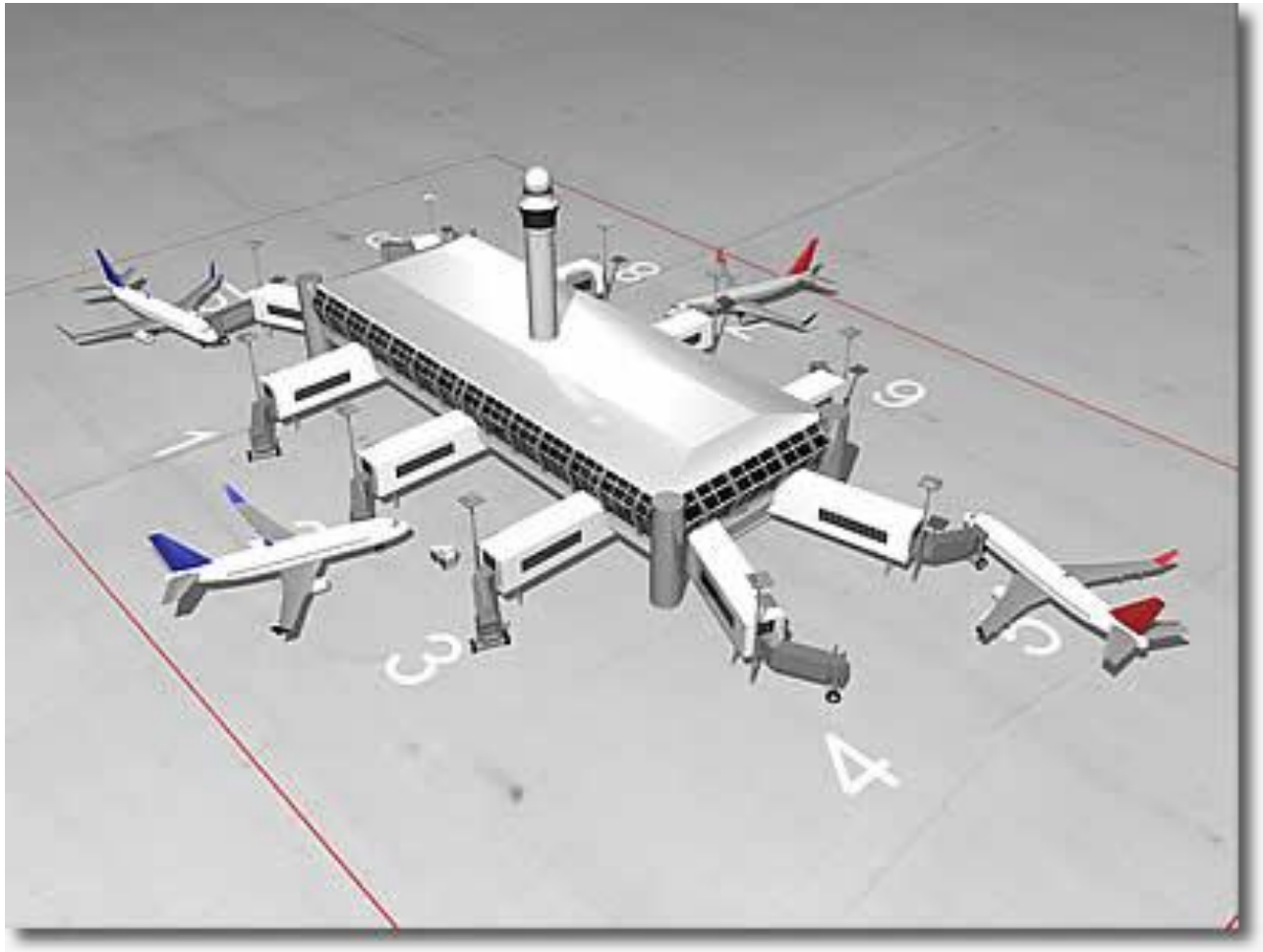
Airport HUB



Agenda

- USB HUB Introduction and Definitions
- USB Speeds and Hub Transaction Translators
- Different power consumptions allowed on USB HUB
- Technical design consideration and debugging
- USB 3.0 HUB
- Microchip USB Hub offering

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USB HUB Introduction and Definitions

A USB hub is a device the expands a single USB port into several so that there are more ports available to connect devices to a host system.

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Definitions

- **Upstream Port** – The port a USB Hub that faces the USB Host
- **Downstream Ports** – The Ports on the USB Hub that faces the USB devices
- **Self-Powered** – Powered by a power supply that connects directly to the USB device or Hub.
- **Bus-Powered** – Powered by the USB Connector VBUS pin.
- **Configured/Unconfigured** – A USB device is Unconfigured at first connection until the Host has assigned an address and enabled it. After this point the device is considered to be Configured

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Definitions

Non-Removable Ports

Ports which contain non-removable devices (permanently attached to the HUB)

- Windows testing will fail if non-removable ports are not declared
- Non-removable Devices must be attached to the lowest numbered ports
- Strapping options, SMBus/I²C™ or external EEPROM configurations allow all ports to be non-removable
- Strapping any ports as non-removable also causes the hub to declare itself as part of a compound device

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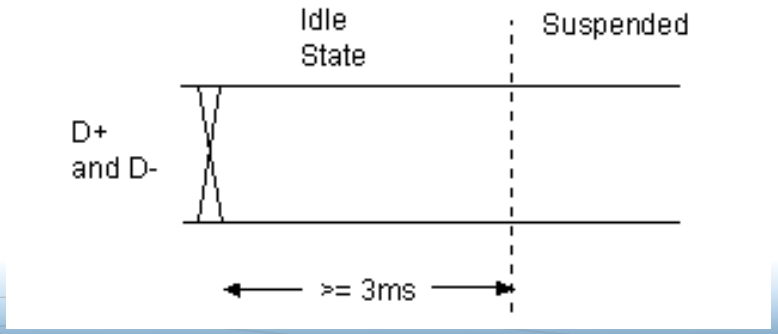
Definitions

- **USB Compound device**
  - Allows a Mix of USB HUB and USB Functions
  - Use a Single Connection to the Host
  - Can add User-accessible ports
- **USB Suspend states**
  - "Enabled" hub downstream port will enter suspend state when….
    - **Hub receives port suspend command (Selective Suspend)**
    - **Hub enters global suspend state (3ms of no BUS activities)**



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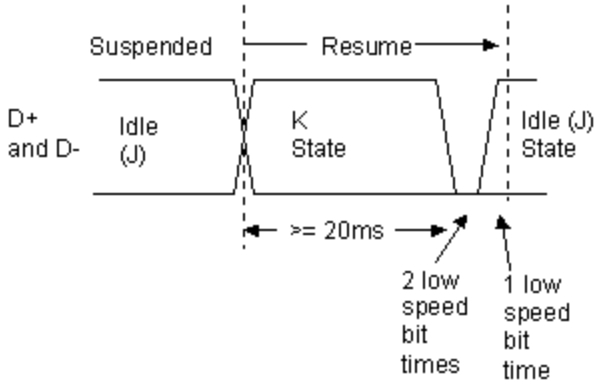
Definitions

USB Resume

- When the host wants to wake the device up after a suspend, it does so by reversing the polarity of the signal on the data lines for at least 20ms.



- It is also possible for a device with its remote wakeup feature set, to initiate a resume itself (15ms Kstate)

- Once resumed ….Port returns to “enabled” state

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USB Speeds

USB1.1

- **Low Speed (1.5 Mbps) Devices:**
  - Signal Low Speed operation by enabling 1.5K pull-up Resistor on D-
- **Full Speed (12 Mbps) Devices:**
  - Signal Full Speed operation by enabling 1.5K pull-up Resistor on D+

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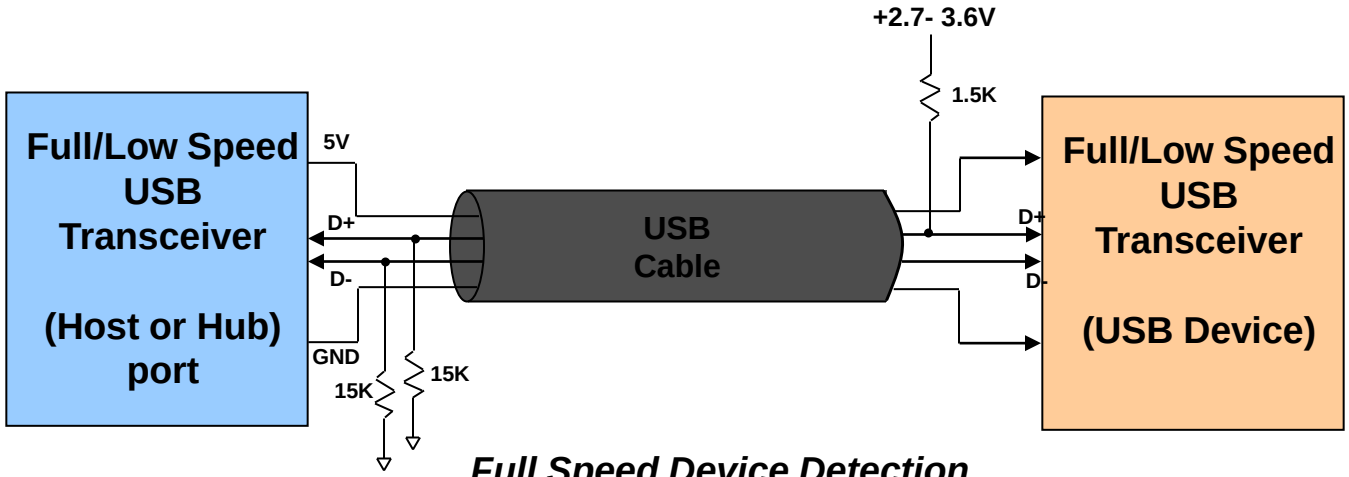
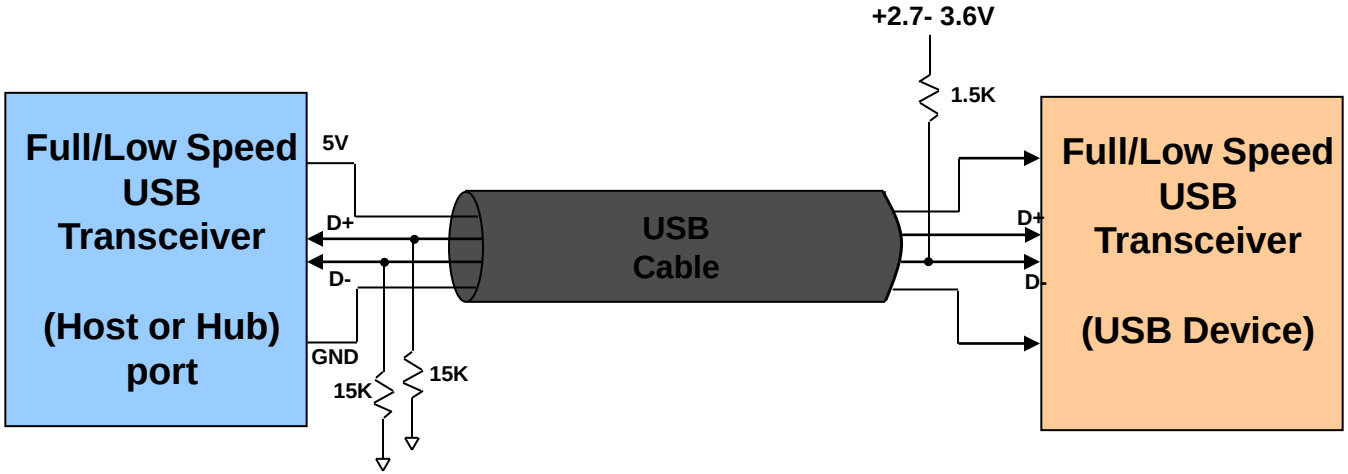
USB Attachment and Speed Detection



Full Speed Device Detection



Low Speed Device Detection

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USB Speeds

USB2.0

- **High Speed (480 Mbps) Devices:**
  - Signal High Speed operation via the speed negotiation (“Chirp detection”)

USB3.0

- **Super Speed (5 Gbps) Devices:**
  - Use a complete different data path (TX+, TX- and RX+, RX-) to perform USB3.0 communication

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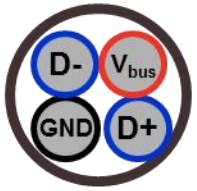
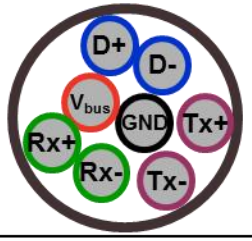
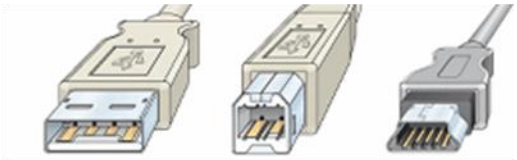
USB Speeds

USB1.1	USB 2.0	USB 3.0
12Mbps	480 Mbps	5 Gbps
4 wires 		8 wires 
Up to 5-meter cable		Up to 3-meter cable
Standard A, B, AB connector 		Backward compatible with standard A/B, new micro B/AB connector

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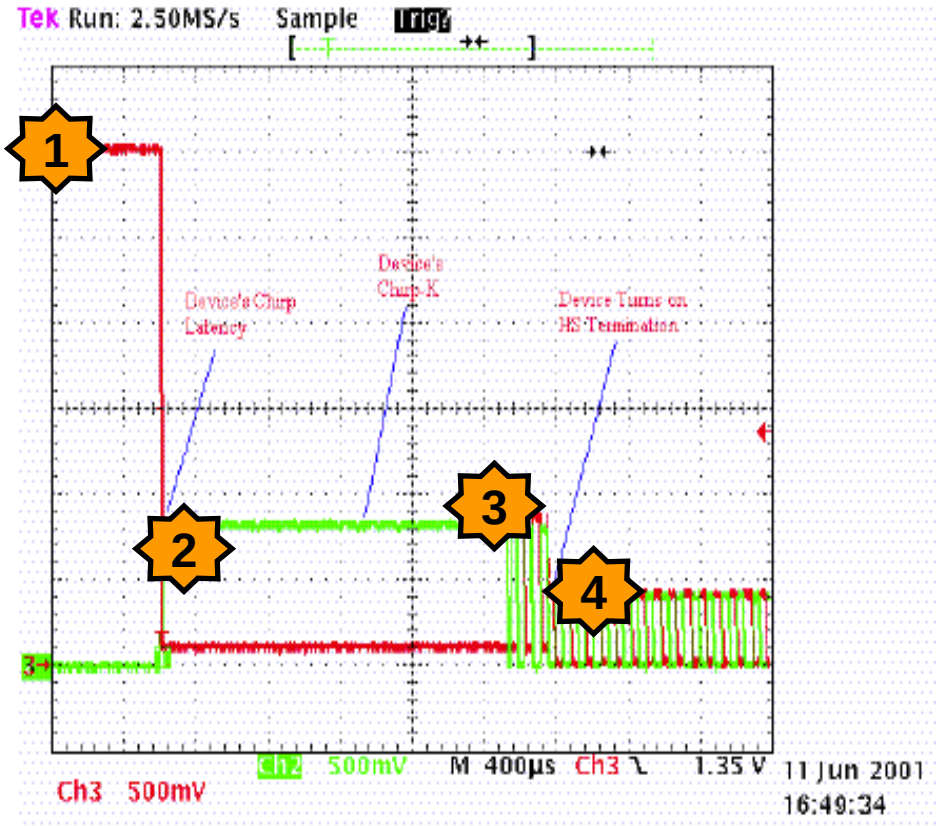
Negotiation for High Speed

Chirp and speed detection

- **1** - Device starts by attaching as Full Speed (1.5K Pullup on D+)
- **2**- HOST send a USB reset and the Device then issues a Chirp K, driving HS current (~18 mA) into the upstream 45 Ohm Termination resulting in ~800mV on D-
- **3** - High Speed Host / Downstream USB Hub Port response is Chirp JK sequence
  - Alternating HS current driven into D+ and D-
  - Full Speed Host/Downstream Hub will Ignore the Device's Chirp K
- **4** - Device applies High Speed termination
  - Signal Amplitude drops to ~400 mV



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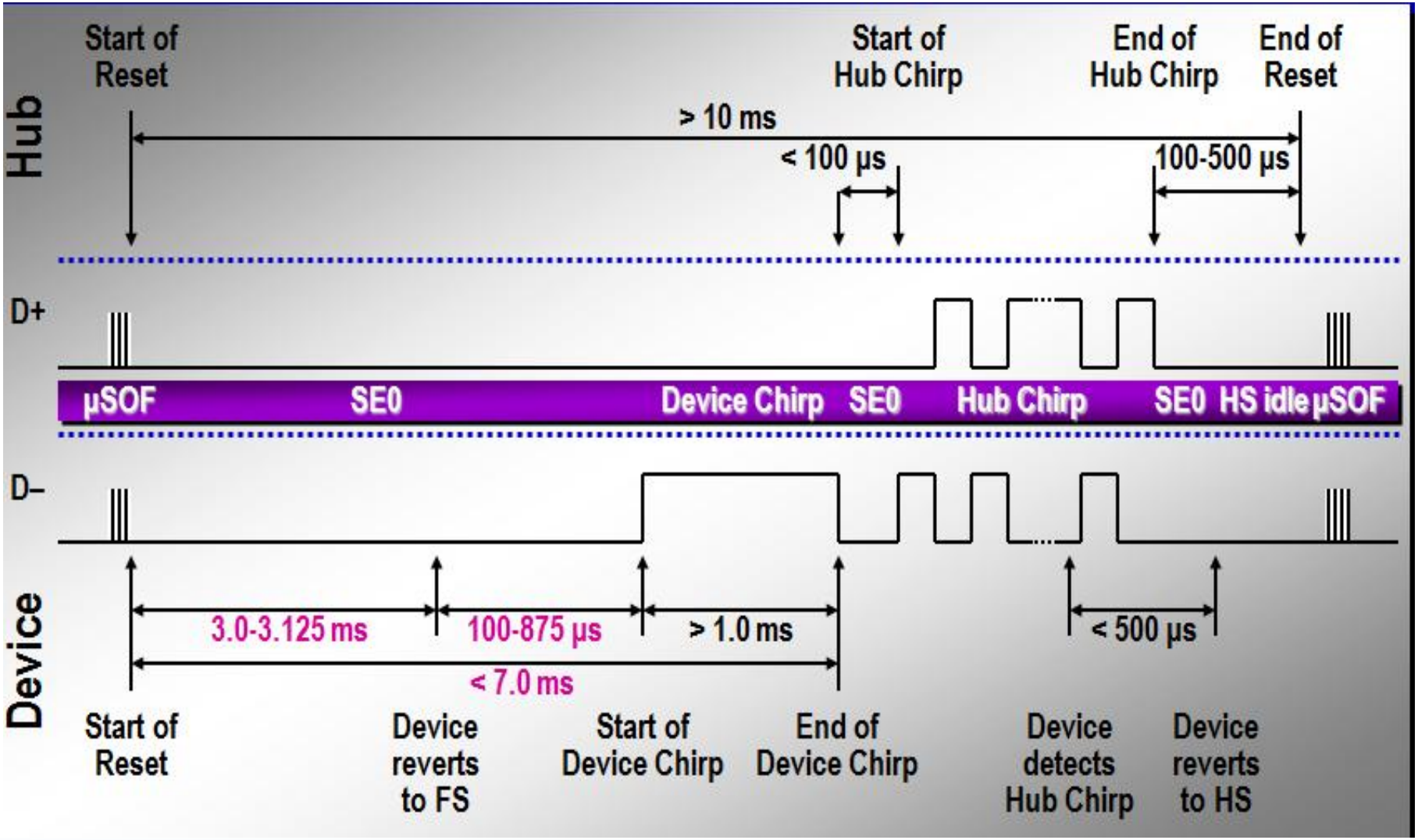
USB 2.0 speed detection



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USB Addressing

- **USB Devices are assigned addresses from 0 to 127 (decimal)**
  - All Devices (including hubs) respond at address 0 following Power On or Reset
  - After Reset, all Hub Downstream Ports are Disabled.
    - **Host only enables one Hub port at a time so that only one device can respond to address 0.**
  - Host assigns a Unique address to each Device.

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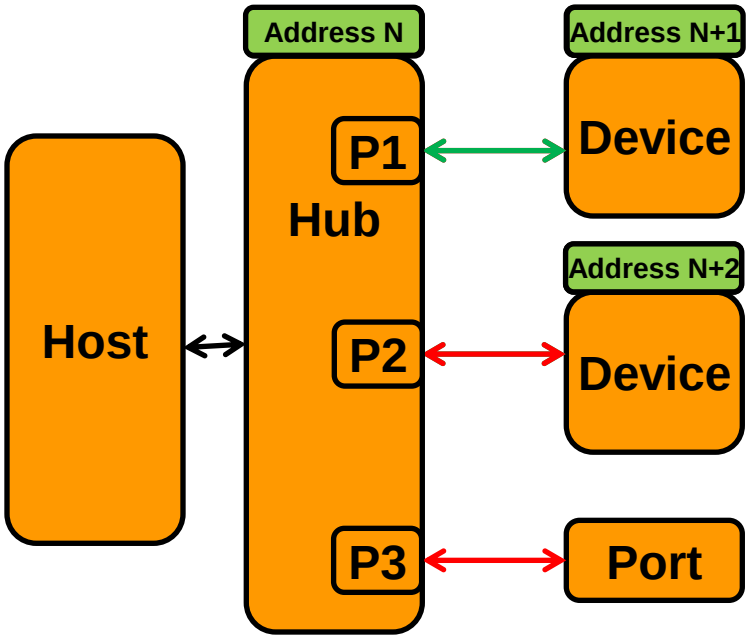
Addressing Devices Attached to Hub

- **Host begins by assigning Hub to Address N**
  - Host Enables Port Power on Port #1
    - **If a device is attached, it is assigned an address (N+1, for example).**
  - This procedure is repeated for all downstream ports



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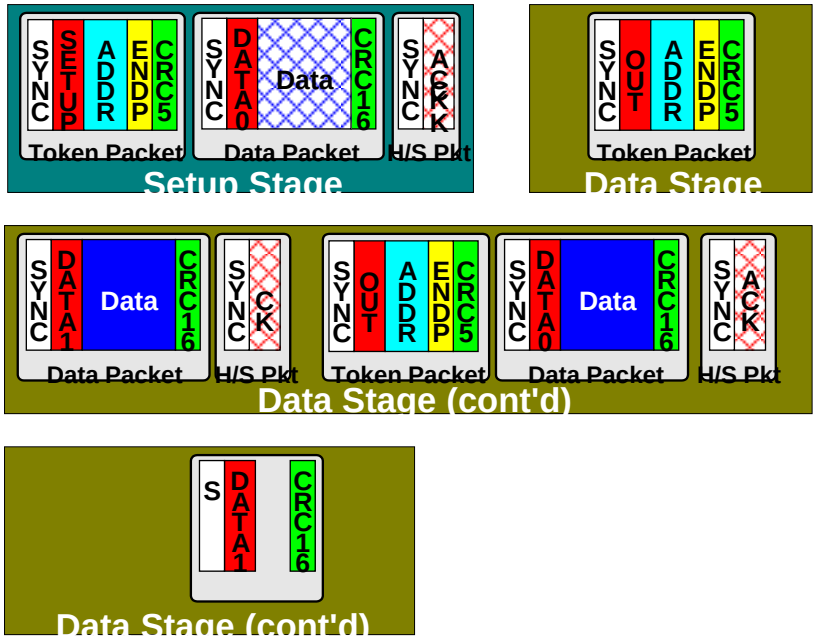
USB HUB Endpoints

By spec the USB HUB utilizes two type of USB transfers/endpoints

- **"Control Endpoint" for enumeration**



A Control Write Transfer

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USB HUB Endpoints

Interrupt Endpoint" used to control the status of the HUB through the HUB and port Status Change bitmap

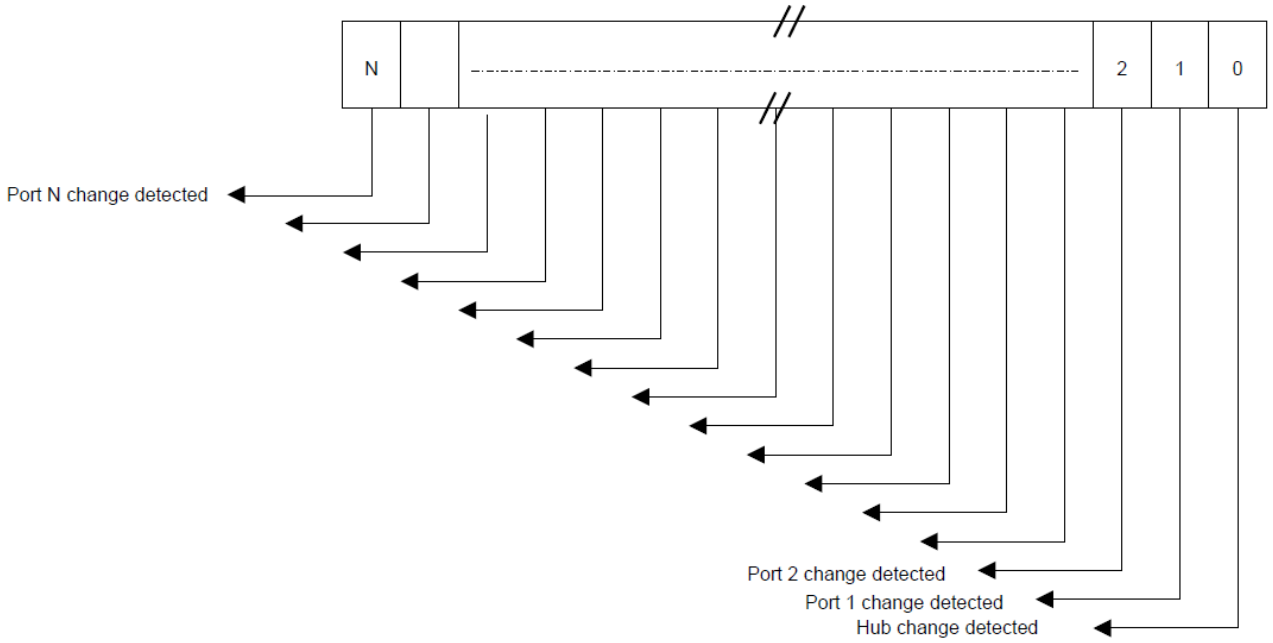

Figure 11-22. Hub and Port Status Change Bitmap

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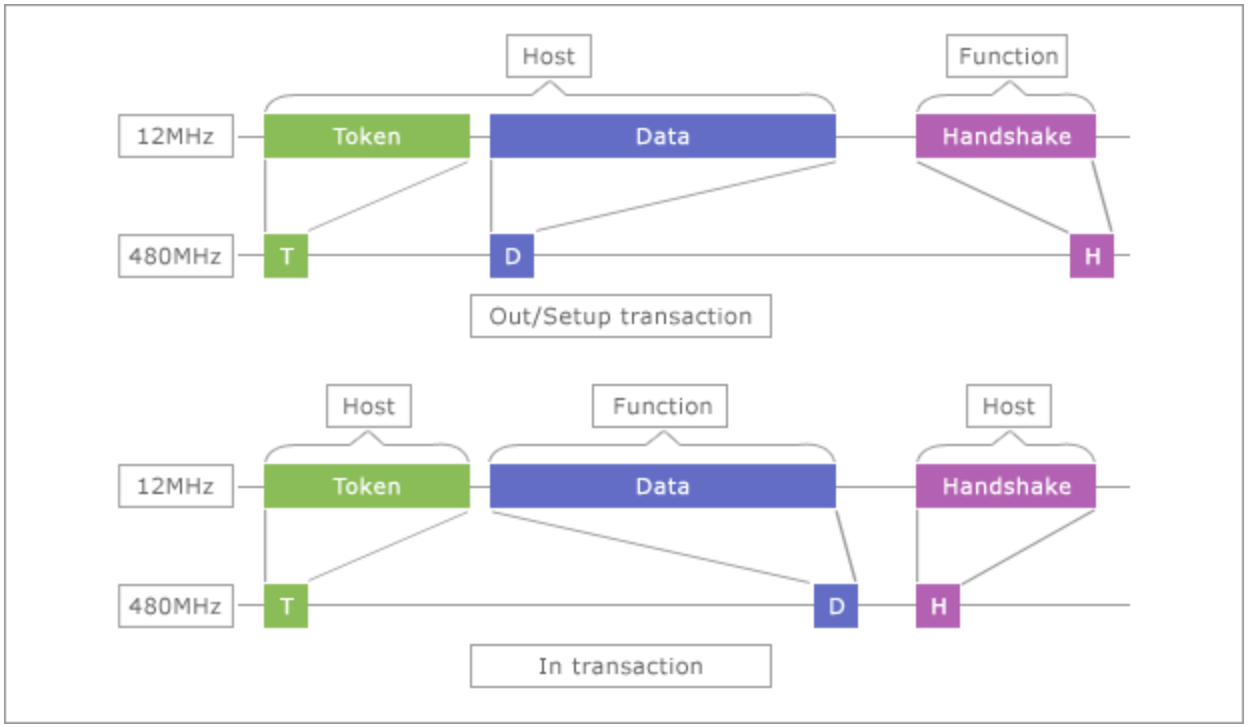
USB transactions



USB 2.0 is designed to allow data communication at 480Mbps while maintaining compatibility to USB1.1 12 Mbps

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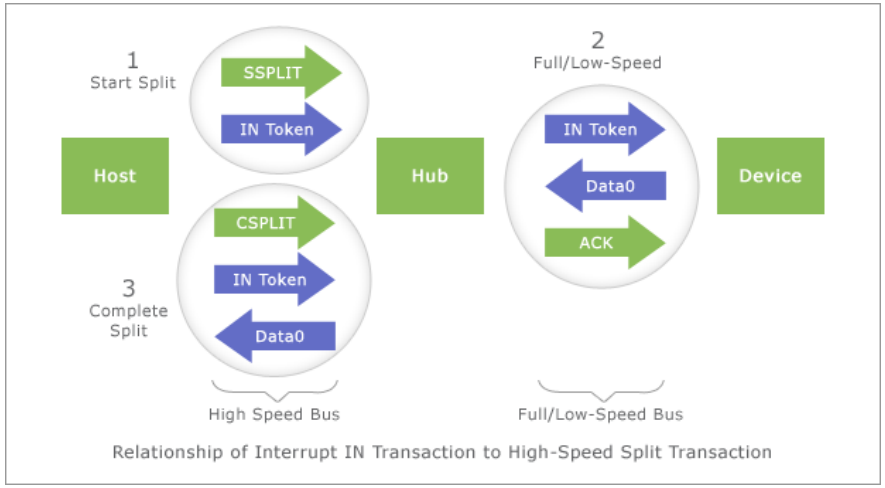
USB2.0 Split Transactions

2 types of split transactions:



Split transactions are the means by which the hub handles Low or Full speed traffic on the downstream ports without degrading the upstream High Speed bus performance.

The transaction is “Split” into phases; a Start Split and a Complete Split.

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Transaction Translators

A Transaction Translator (TT) acts as a buffer between a High-Speed Host and a Full-Speed or Low-Speed Device.

- Upstream, the Host Reads and Writes to the TT at High-Speed. Downstream, the TT transfers Data to the Device at Full or Low-Speed.
- USB Hubs contain a minimum of One TT. Multi-TT Hubs contain one TT per Downstream Port

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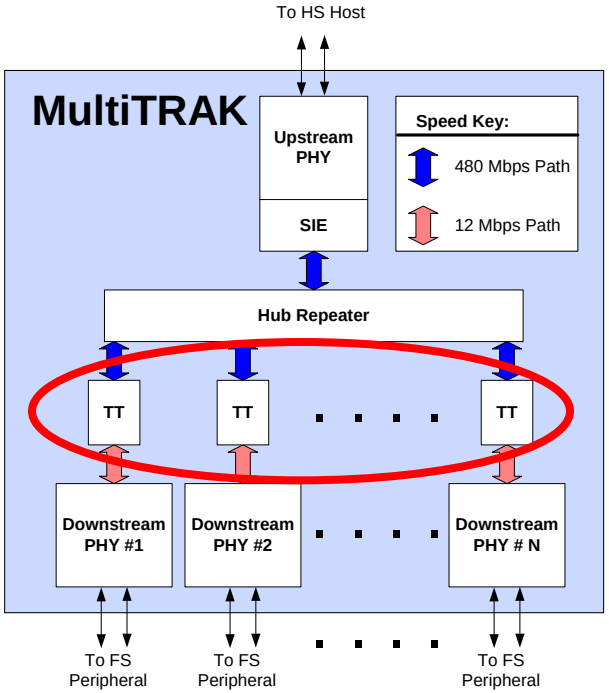
MultiTRAK™ eliminates FS traffic congestion

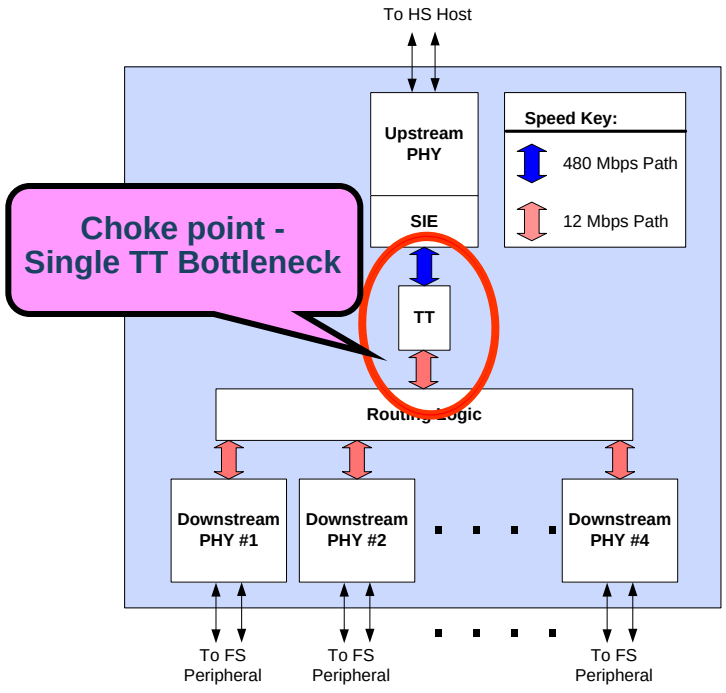
SMSC USB2.0 Hubs*
With MultiTRAK



*** Exclude USB2502**

- **One TT per Port**
- **"Dedicated" 12 Mbps pipe for every downstream FS/LS device**

Other USB 2.0 Hubs



- **One TT per Hub**
- **A single 12 Mbps pipe "shared" among 4 downstream FS/LS devices**

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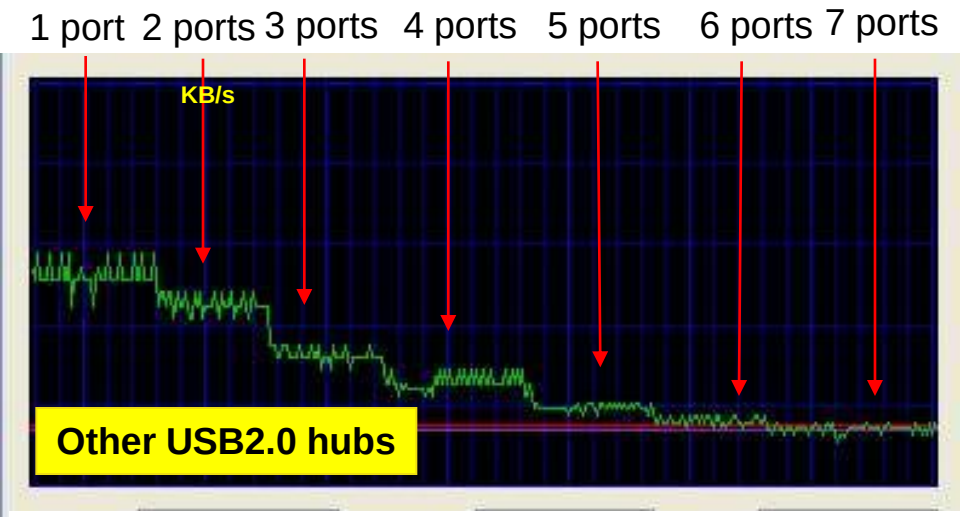
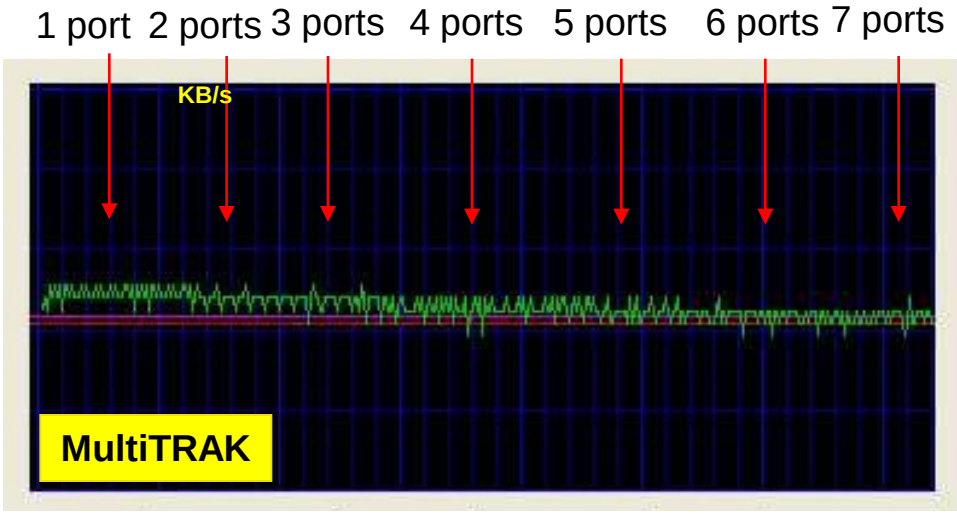
MultiTRAK™ provides highest FS data throughput

- **MultiTRAK hubs guarantee maximum FS Bulk Read/Write throughput for EVERY downstream port**





- **MultiTRAK is 2x faster than single-TT with 4 FS bulk traffic**
- **MultiTRAK is 3x faster than single-TT with 7 FS bulk traffic**

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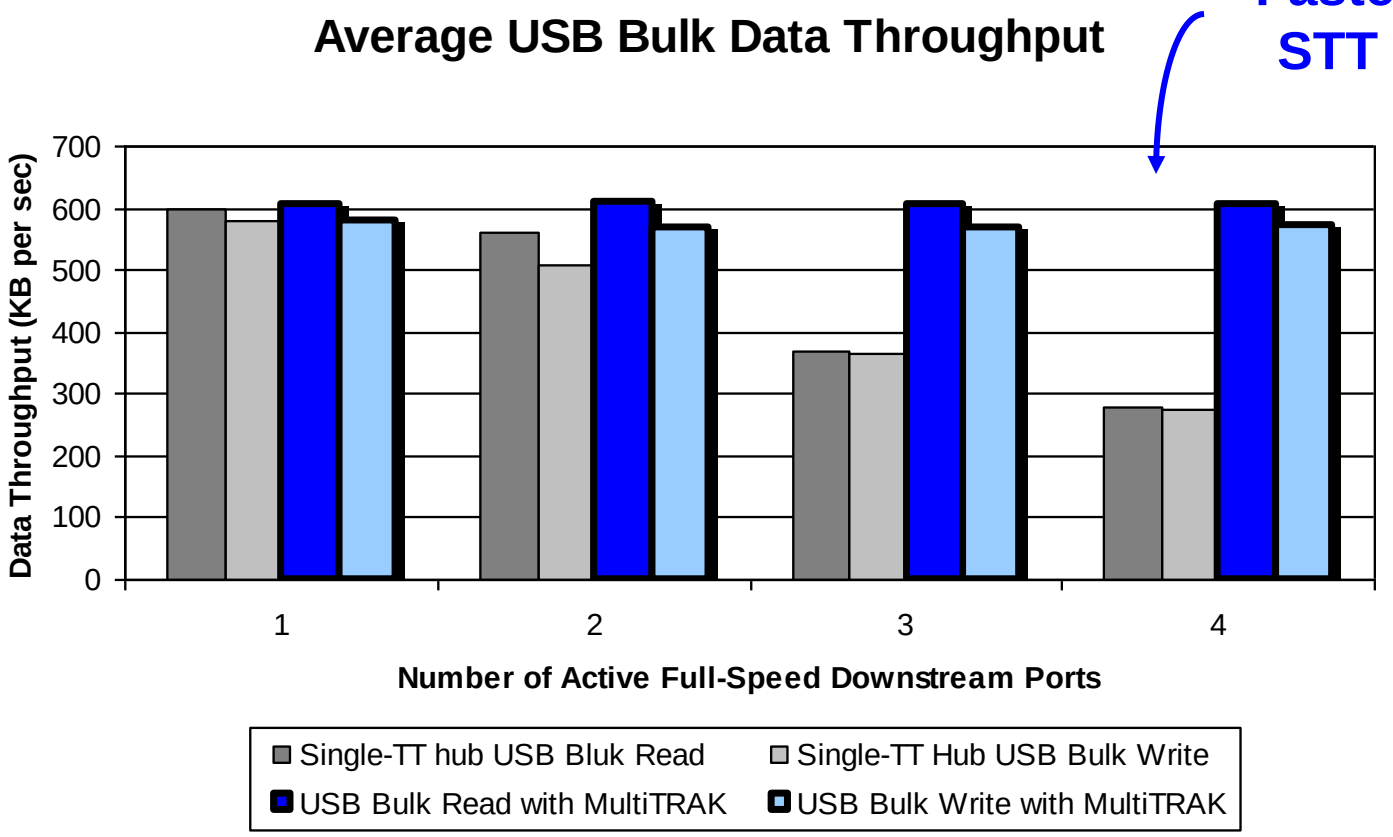
MultiTRAK™ provides highest FS data throughput

MTT hubs guarantee maximum FS Bulk Read/Write throughput for EVERY downstream port

Up to 200% Faster than STT hubs



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Power Considerations

- **Bus Powered HUB**
  - **Unconfigured**: (Total) < 100 mA
  - **Configured**: < 500 mA
    - HUB Current + 100mA * (# of DP)
    - Downstream Ports can not support 500 mA
    - 2 USB Bus Powered HUB in cascade are not allowed by spec
- **Self Powered**
  - (Total) < 100 mA

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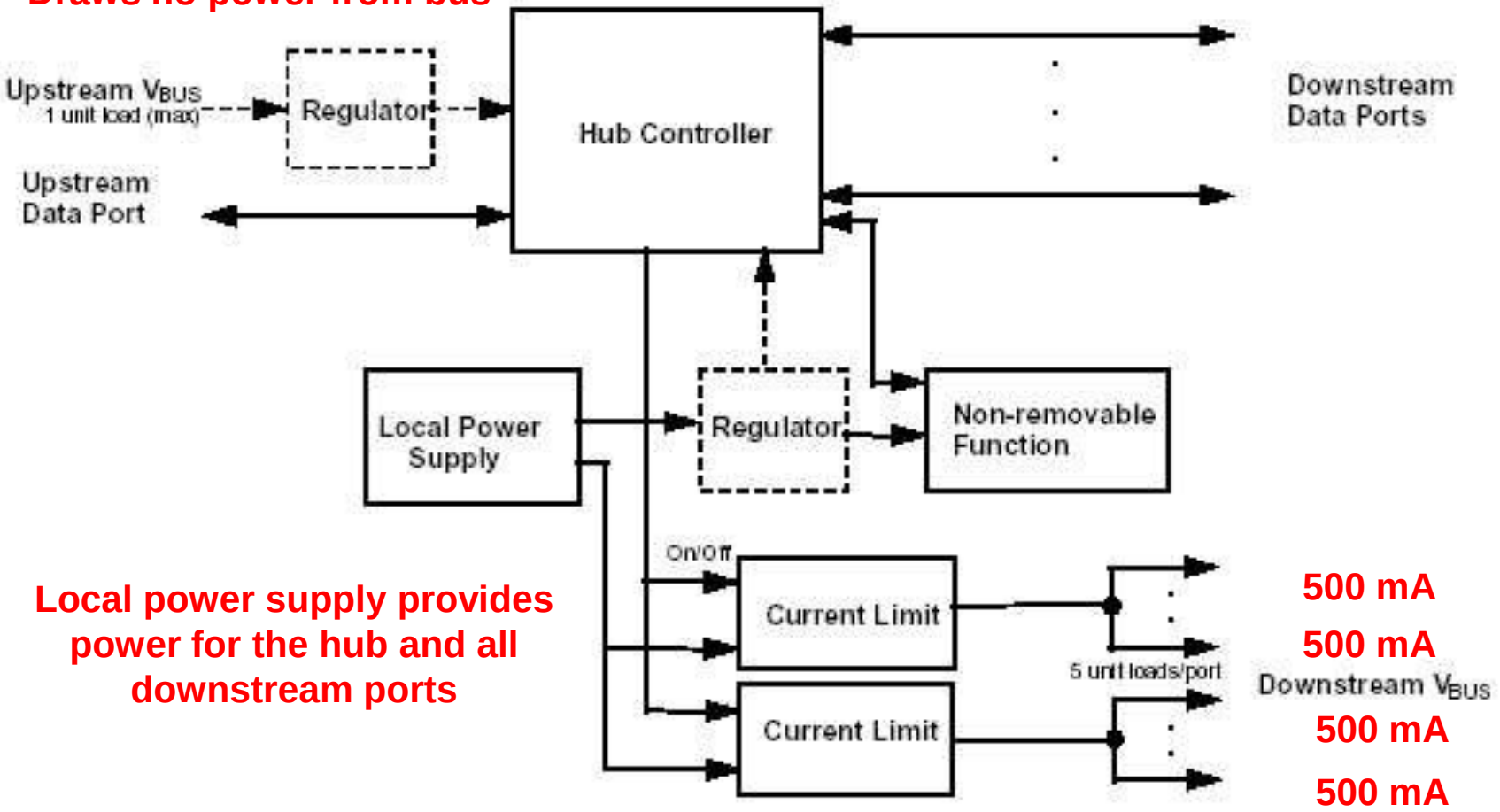
USB Power Management Policy

Self-powered hub

Draws no power from bus



Local power supply provides power for the hub and all downstream ports

Figure 7-43. Compound Self-powered Hub

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USB Power Management Policy

Bus-powered hub

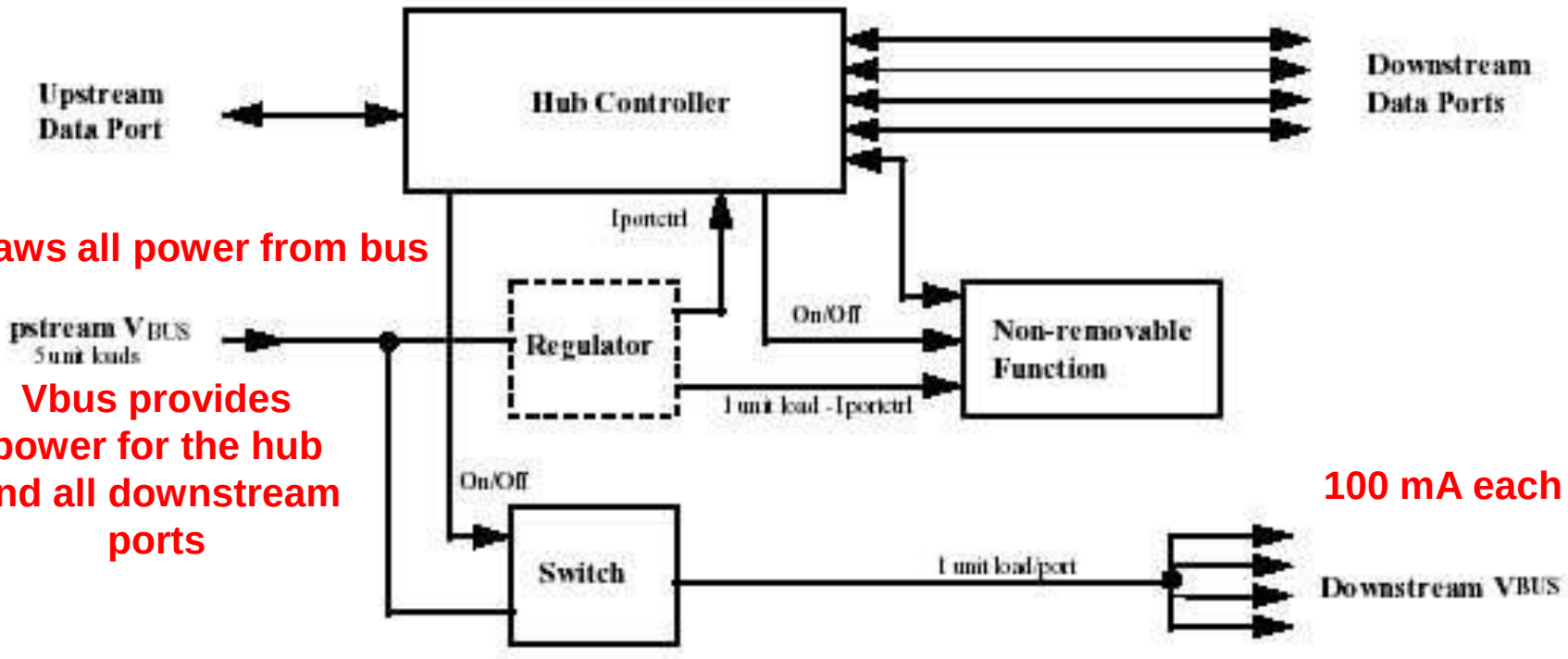

Figure 7-42. Compound Bus-powered Hub

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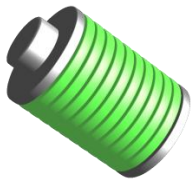
The Changing USB Universe

The USB Eco system continues to increase in capability's in both Speed and Power

- Faster speeds 1.5Mbs, 12Mbs, 480Mbs, 5Gbs
- Higher power – 500ma, 900ma, 1500ma, 100W
  - **Power Delivery is coming soon – 2013!**
- Battery Charging standards evolve constantly with both vendor specific and standards based solutions
  - **USB-IF specifications - BC1.1, BC1.2,**
  - **Apple (L/M/H), RIM (Blackberry) "defacto standards"**
  - **China and Europe have adopted countrywide standards**
  - **USB Battery charging (17058 USB5) class available at the MCHP Master**
- The USB-IF compliance tests continually evolve
- Mobile devices are changing the landscape



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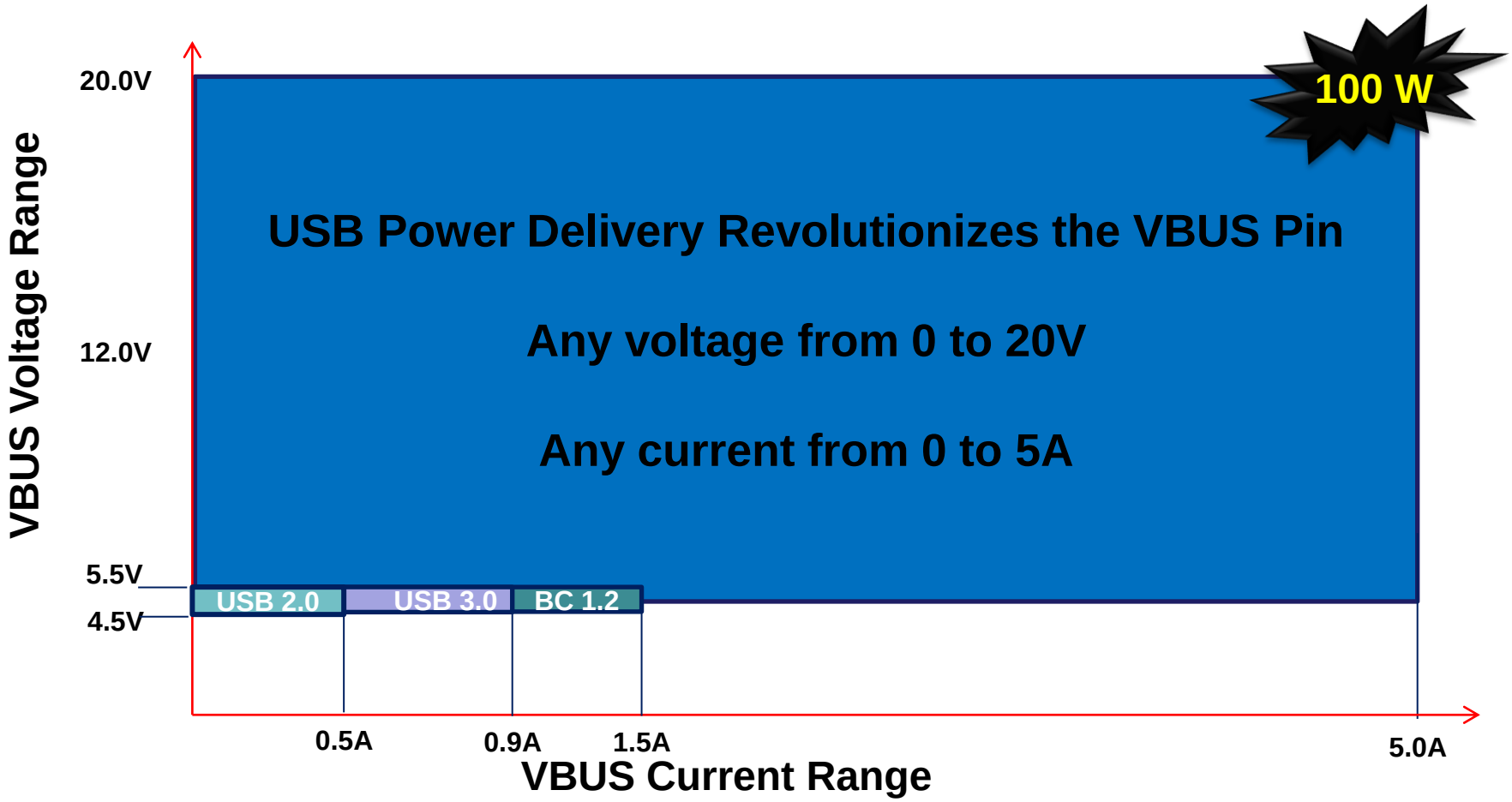
USB VBUS Progression



VBUS Can Now Provide Up To 100W of Power

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Important features to consider when choosing USB HUB

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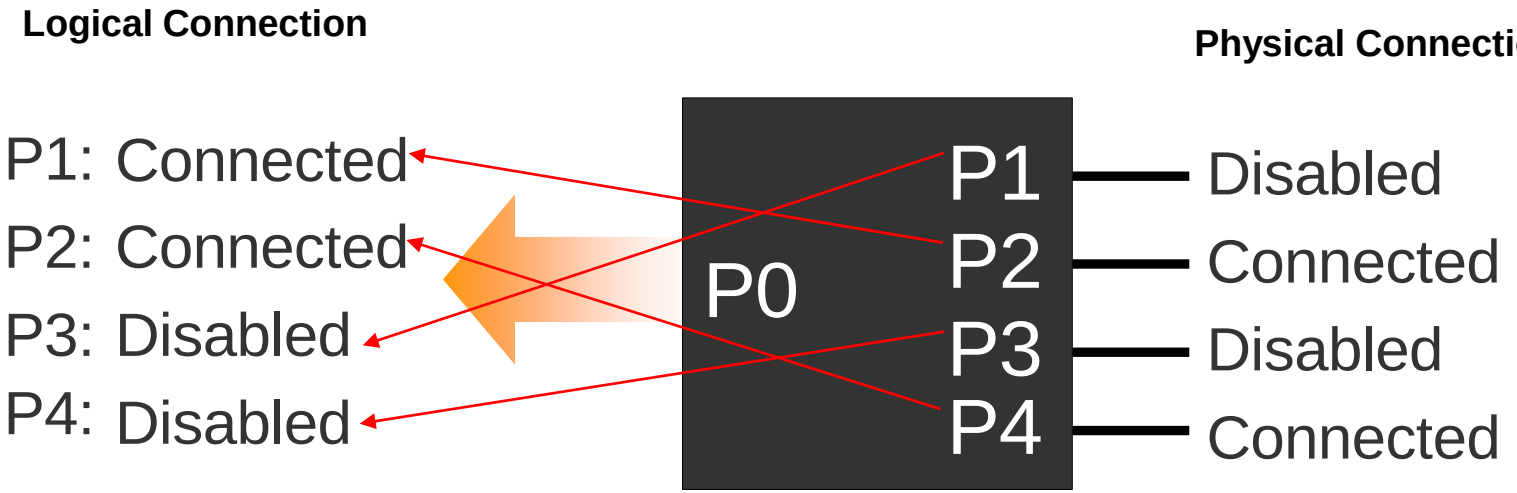
PortMap

PortMap provides flexible port mapping and disable sequence

- For any port that is disabled, USB251x automatically reorder the remaining ports to match the USB host controller's port numbering scheme



USB port virtualization

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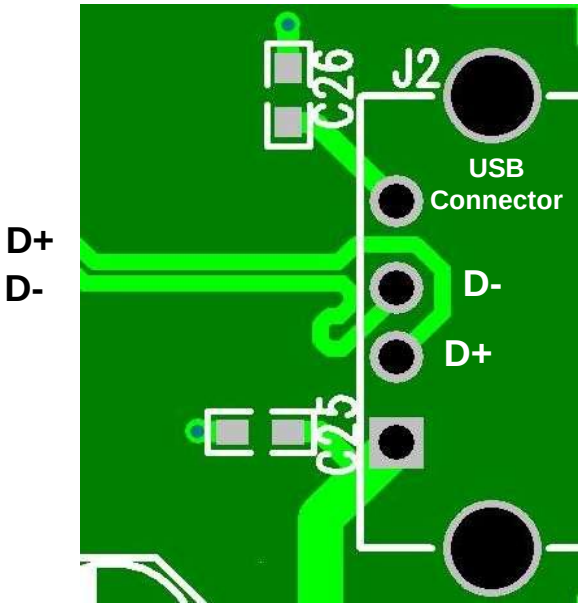
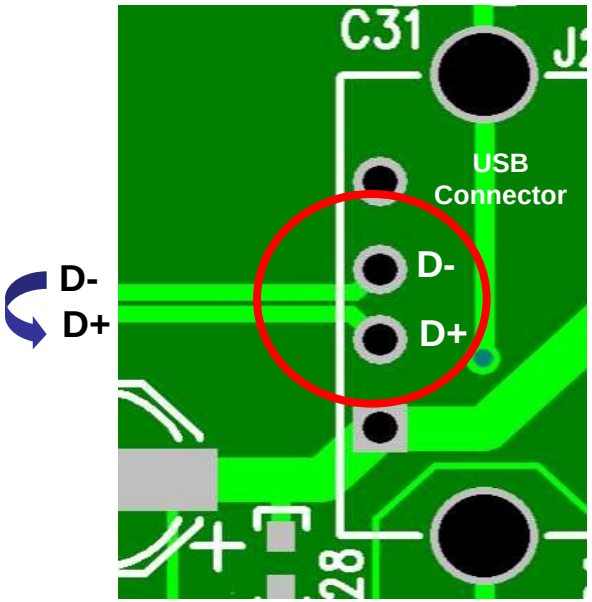
PortSwap

PortSwap adds per-port programmability to USB differential-pair pin location and allows direct alignment of USB signals (D+/D-) to connectors thus avoiding uneven trance length or crossing of the USB differential signals on the PCB





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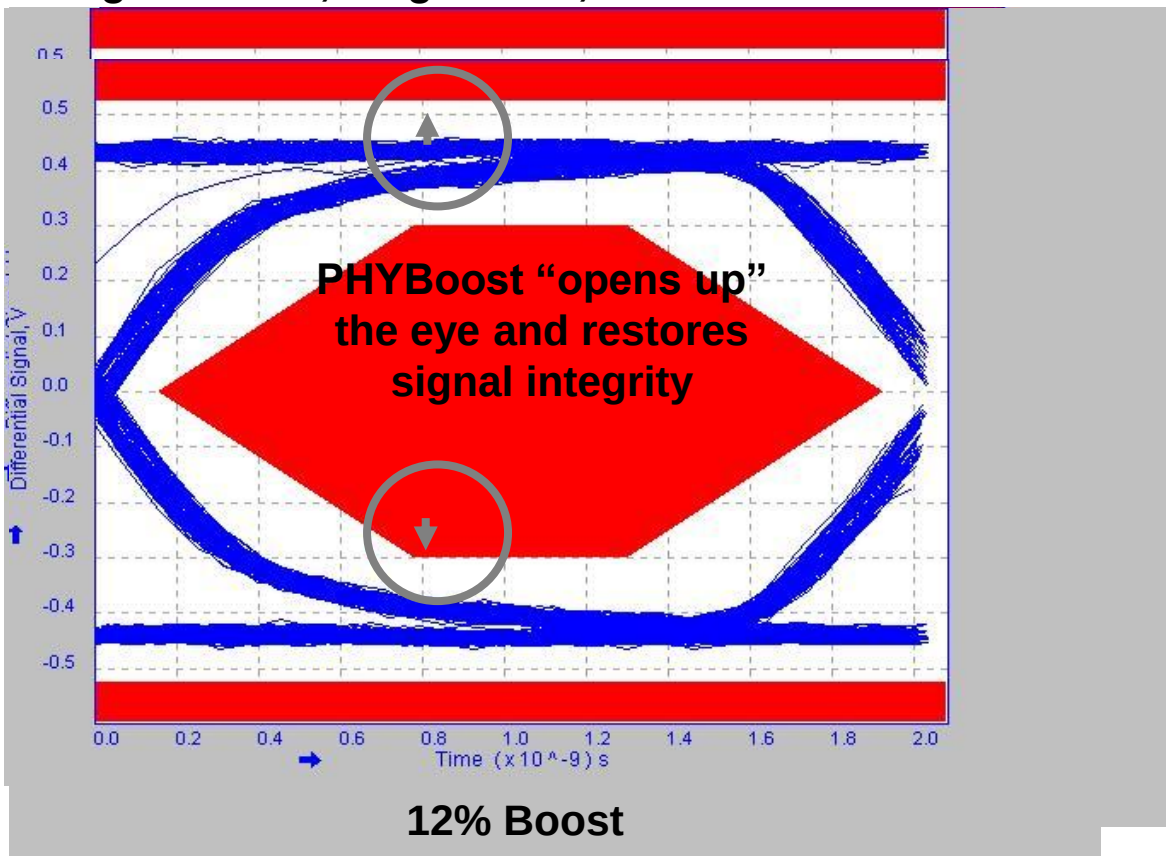
PHYBoost

PHYBoost enables four-level programmable USB signal drive strengths (0%, +4%, +8%, +12%) in downstream port transceivers. PHYBoost attempts to restore USB signal integrity that has been compromised by system level variables such as poor PCB layout, analog switches, long cables, etc.



Eye diagram compromised system environment

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USB 2.0 Hub HW design consideration

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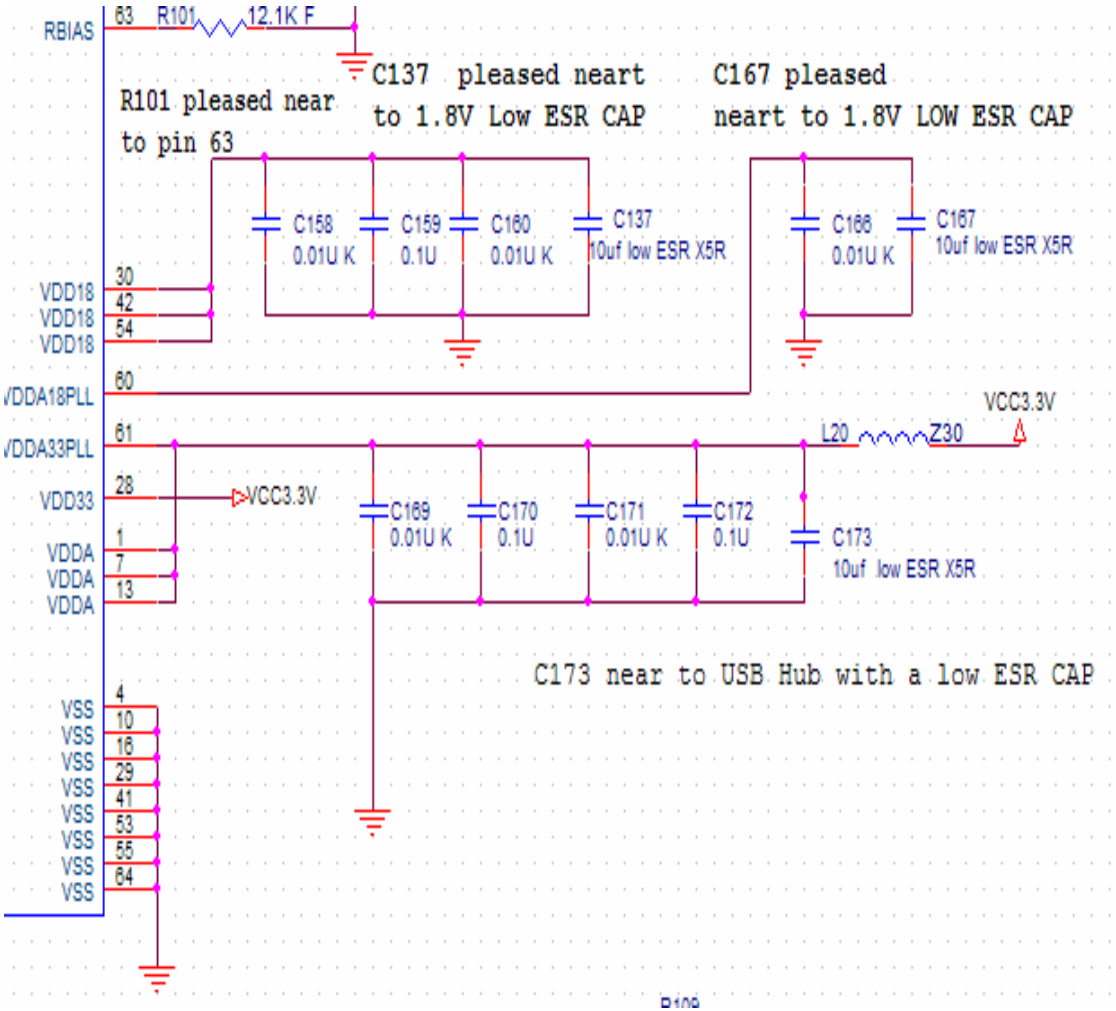
Power Decoupling caps

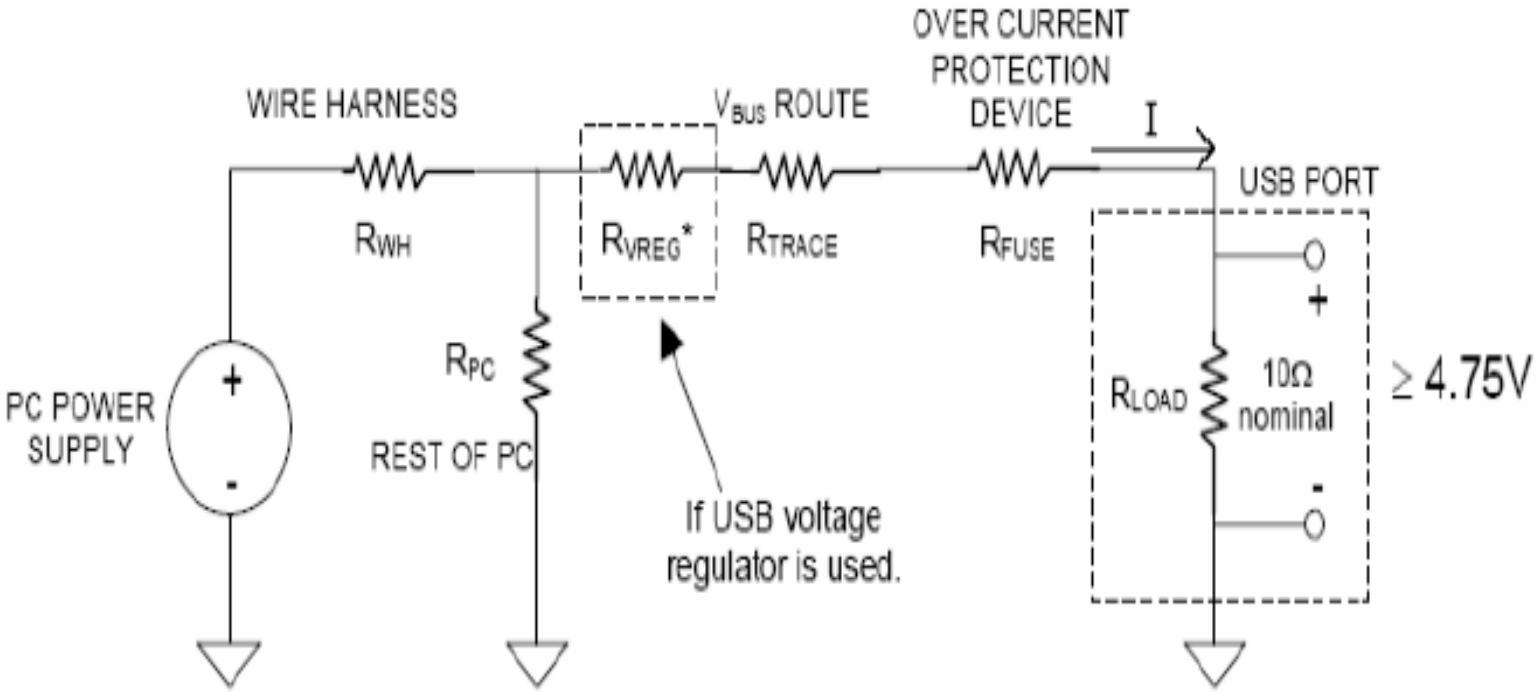
SMSC USB Hubs contain 2 integrated LDO Regulators

- External Low ESR (<200mΩ) Caps are Required



Add the Voltage drop budgeting (Self Power Hub)
The voltage seen at the port must be between 5.25 and 4.75V

$$5.25V \geq V_{PC\_POWER\_SUPPLY} - [(I \times R_{WIRE\_HARNESS}) + (I \times R_{VBUS\_TRACE}) + (I \times R_{V\,REG}) + (I \times R_{FUSE\,ELEMENT})] \geq 4.75V$$



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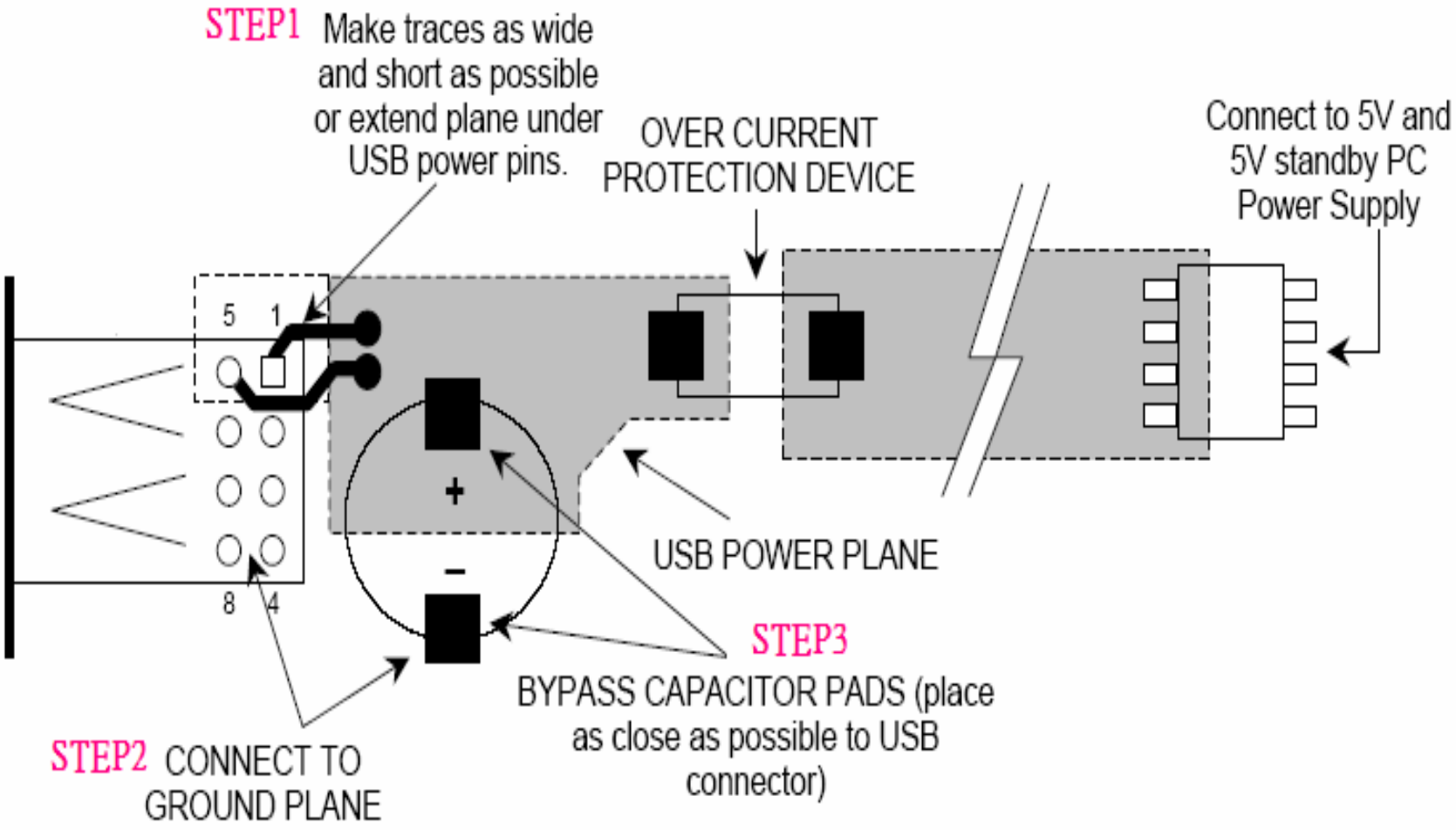
USB +5v VBUS voltage design for the Downstream port


STEP1 Make traces as wide and short as possible or extend plane under USB power pins.
OVER CURRENT PROTECTION DEVICE
Connect to 5V and 5V standby PC Power Supply
5
1
8
4
+
–
USB POWER PLANE
STEP3
BYPASS CAPACITOR PADS (place as close as possible to USB connector)
STEP2 CONNECT TO GROUND PLANE

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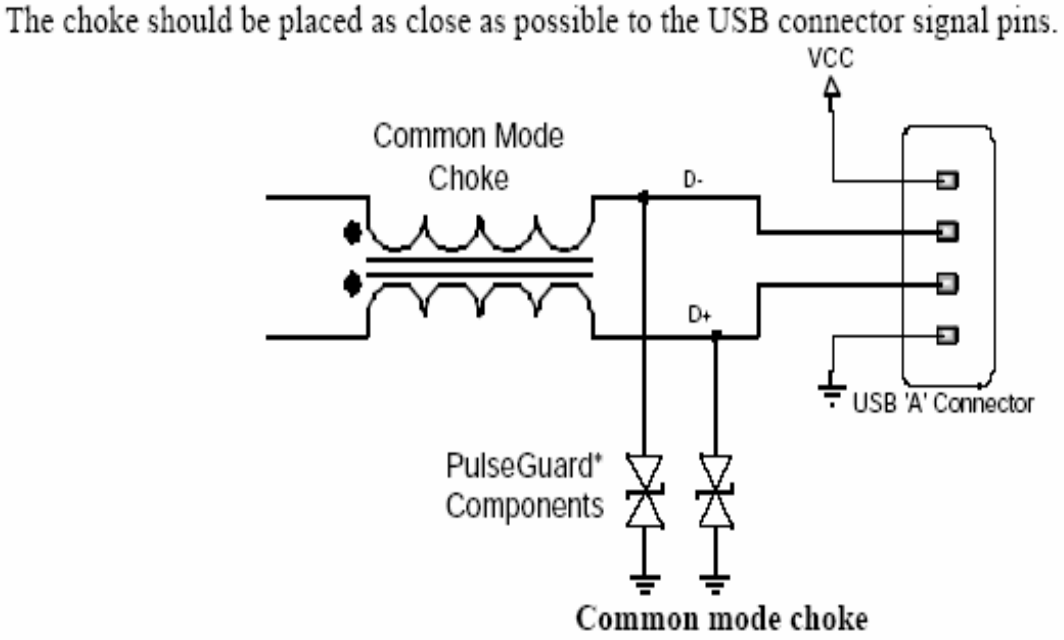
USB EMI/ESD design guide consideration
Typical common choke and suppression component

- **All Common Mode Chokes and ESD Diodes must be specified for a differential impedance of 90Ω for HS USB applications**



- **Always include pad options for resistor bypass of the CMC and de-pop the diodes when possible**

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USB Tech Tips

- HS and SS USB have specific routing requirements that must be followed. See AN 26.2 for more detail.
- USB Hubs can be configured via straps, EEPROM, and I²C™/SMBus. Leave a population option for the default strapping.
- USB Oscillator and some internal regulators are disabled during USB Suspend to save power. If a customer tells you the oscillator is stopping, try connecting to a host.
- Drivers – USB Hubs and Flash Media Readers use the default driver from the OS. No need to download drivers.
- Test Equipment – Low cost USB analyzers available from Teledyne LeCroy/CATC and TotalPhase. Encourage your customer to invest in one.
- EMI and ESD Protection, if improperly specified, can render a USB device inoperable. If present, remove/bypass and re-test.
- RBIAS value must be exactly as specified in the data sheet. Changing this value affects output voltages and input thresholds.

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USB Debug - When enumeration fails without USB traffic

- **Does D+ go to 3V when attaching to host?**
- **Check power**
  - VDD18 should be 1.8V
  - VDD18PLL should be 0V (suspend state) or 1.8V if USB traffic
- **Check hardware reset**
- **Check clock – measure on XTAL2**
- **Check configuration (strapping, EEPROM, SMBus)**
- **Check VBUS_DET pin. USB devices use this pin to signal that the cable to the host is attached.**

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USB Debug - When enumeration fails with USB traffic

- **Full-speed**
  - Check that USB Reset is generated
  - Check that SOFs starts less than 3 mS after end of USB Reset
- **High-speed**
  - Check that USB Reset is generated
  - Check that chirping occurred
  - Check that SOFs starts less than 3 mS after end of USB Reset
- **Collect CATC trace**
  - Check descriptor data returned (configuration)
  - Check for errors (timeouts or CRC)

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USB 2.0 CATC bus analyzer application

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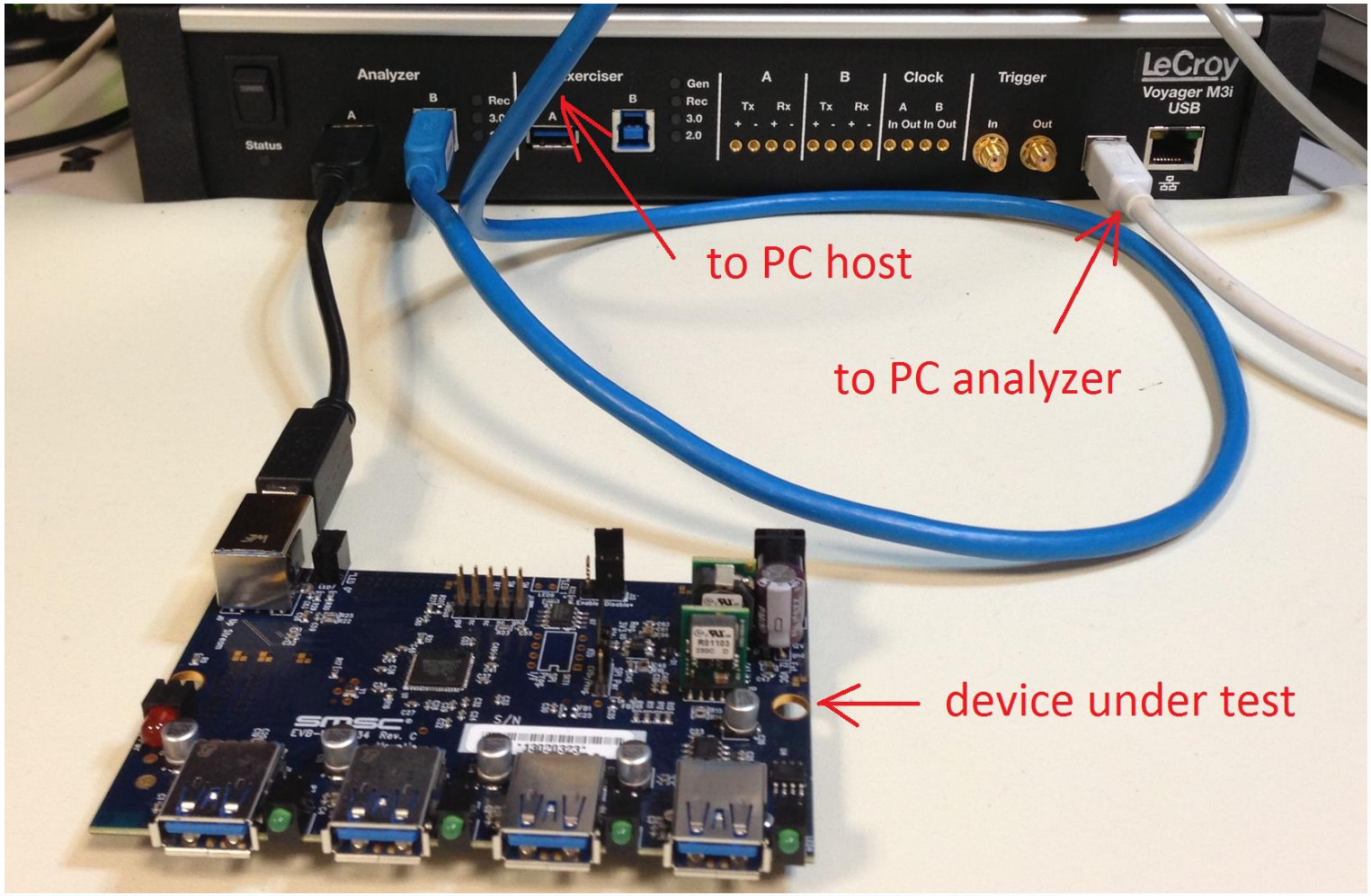
CATC bus analyzer



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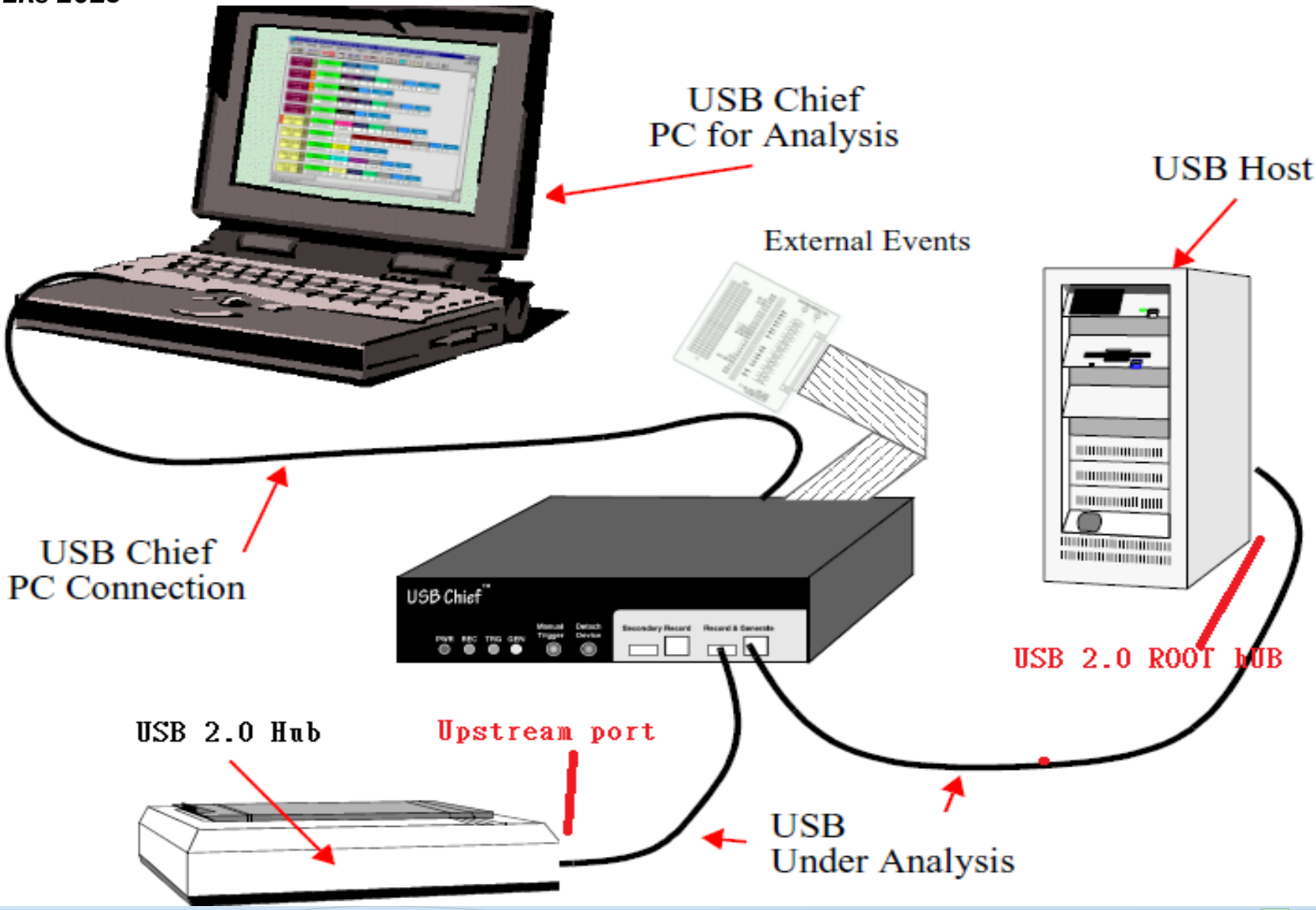
CATC bus analyzer connection



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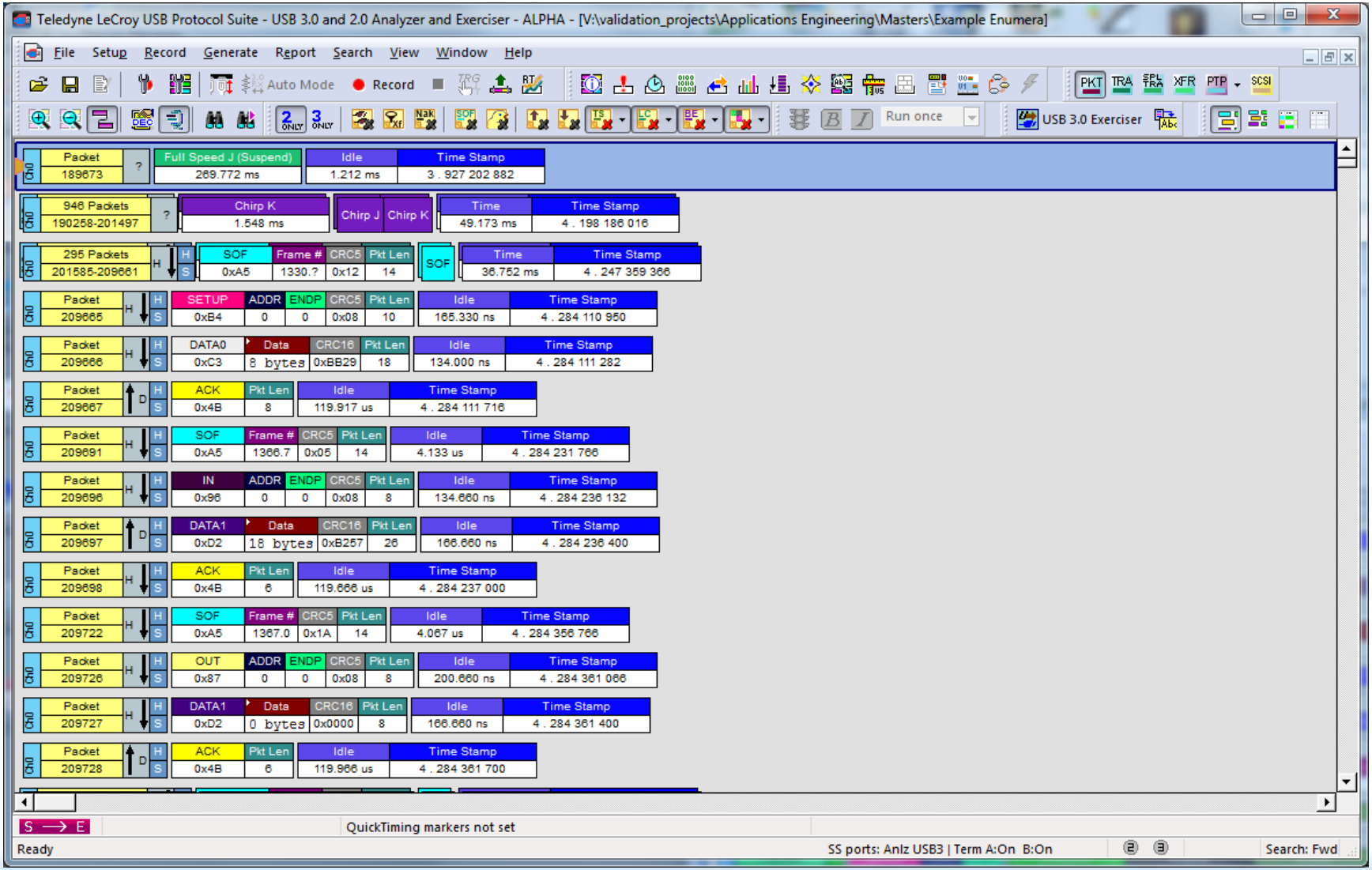
LeCroy Analyzer Screenshots


Teledyne LeCroy USB Protocol Suite - USB 3.0 and 2.0 Analyzer and Exerciser - ALPHA - [V:\validation_projects\Applications Engineering\Masters\Example Enumera]
File Setup Record Generate Report Search View Window Help
Auto Mode Record Run once USB 3.0 Exerciser
Packet 189673 | Full Speed J (Suspend) 269.772 ms | Idle 1.212 ms | Time Stamp 3 . 927 202 882
946 Packets 190258-201497 | Chirp K 1.548 ms | Chirp J | Chirp K | Time 49.173 ms | Time Stamp 4 . 198 186 016
295 Packets 201585-209661 | SOF 0xA5 | Frame # 1330.? | CRC5 0x12 | Pkt Len 14 | SOF | Time 36.752 ms | Time Stamp 4 . 247 359 366
Packet 209665 | SETUP 0xB4 | ADDR 0 | ENDP 0 | CRC5 0x08 | Pkt Len 10 | Idle 165.330 ns | Time Stamp 4 . 284 110 950
Packet 209666 | DATA0 0xC3 | Data 8 bytes | CRC16 0xBB29 | Pkt Len 18 | Idle 134.000 ns | Time Stamp 4 . 284 111 282
Packet 209667 | ACK 0x4B | Pkt Len 8 | Idle 119.917 us | Time Stamp 4 . 284 111 716
Packet 209691 | SOF 0xA5 | Frame # 1366.7 | CRC5 0x05 | Pkt Len 14 | Idle 4.133 us | Time Stamp 4 . 284 231 766
Packet 209696 | IN 0x96 | ADDR 0 | ENDP 0 | CRC5 0x08 | Pkt Len 8 | Idle 134.660 ns | Time Stamp 4 . 284 236 132
Packet 209697 | DATA1 0xD2 | Data 18 bytes | CRC16 0xB257 | Pkt Len 26 | Idle 166.660 ns | Time Stamp 4 . 284 236 400
Packet 209698 | ACK 0x4B | Pkt Len 6 | Idle 119.666 us | Time Stamp 4 . 284 237 000
Packet 209722 | SOF 0xA5 | Frame # 1367.0 | CRC5 0x1A | Pkt Len 14 | Idle 4.067 us | Time Stamp 4 . 284 356 766
Packet 209726 | OUT 0x87 | ADDR 0 | ENDP 0 | CRC5 0x08 | Pkt Len 8 | Idle 200.660 ns | Time Stamp 4 . 284 361 066
Packet 209727 | DATA1 0xD2 | Data 0 bytes | CRC16 0x0000 | Pkt Len 8 | Idle 166.660 ns | Time Stamp 4 . 284 361 400
Packet 209728 | ACK 0x4B | Pkt Len 6 | Idle 119.966 us | Time Stamp 4 . 284 361 700
S → E
QuickTiming markers not set
Ready
SS ports: Anlz USB3 | Term A:On B:On
Search: Fwd

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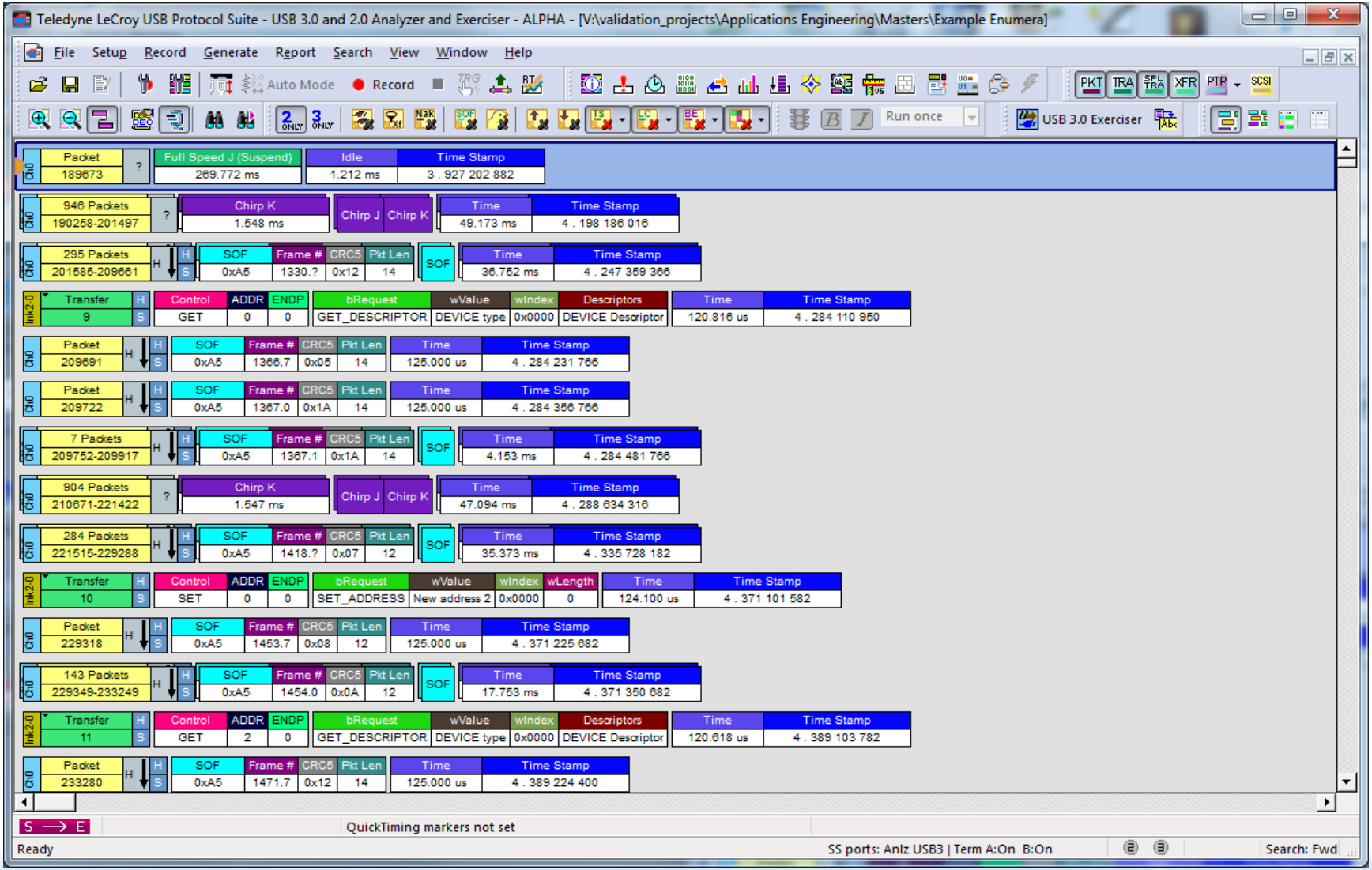
LeCroy Analyzer Screenshots, cont.


Teledyne LeCroy USB Protocol Suite - USB 3.0 and 2.0 Analyzer and Exerciser - ALPHA - [V:\validation_projects\Applications Engineering\Masters\Example Enumera]
File Setup Record Generate Report Search View Window Help
Auto Mode Record Run once USB 3.0 Exerciser
Packet 189673 | Full Speed J (Suspend) 269.772 ms | Idle 1.212 ms | Time Stamp 3 . 927 202 882
946 Packets 190258-201497 | Chirp K 1.548 ms | Chirp J Chirp K | Time 49.173 ms | Time Stamp 4 . 198 186 016
295 Packets 201585-209661 | SOF 0xA5 | Frame # 1330.? | CRC5 0x12 | Pkt Len 14 | SOF | Time 36.752 ms | Time Stamp 4 . 247 359 366
Transfer 9 | Control GET | ADDR 0 | ENDP 0 | bRequest GET_DESCRIPTOR | wValue DEVICE type | wIndex 0x0000 | Descriptors DEVICE Descriptor | Time 120.816 us | Time Stamp 4 . 284 110 950
Packet 209691 | SOF 0xA5 | Frame # 1366.7 | CRC5 0x05 | Pkt Len 14 | Time 125.000 us | Time Stamp 4 . 284 231 766
Packet 209722 | SOF 0xA5 | Frame # 1367.0 | CRC5 0x1A | Pkt Len 14 | Time 125.000 us | Time Stamp 4 . 284 356 766
7 Packets 209752-209917 | SOF 0xA5 | Frame # 1367.1 | CRC5 0x1A | Pkt Len 14 | SOF | Time 4.153 ms | Time Stamp 4 . 284 481 766
904 Packets 210671-221422 | Chirp K 1.547 ms | Chirp J Chirp K | Time 47.094 ms | Time Stamp 4 . 288 634 316
284 Packets 221515-229288 | SOF 0xA5 | Frame # 1418.? | CRC5 0x07 | Pkt Len 12 | SOF | Time 35.373 ms | Time Stamp 4 . 335 728 182
Transfer 10 | Control SET | ADDR 0 | ENDP 0 | bRequest SET_ADDRESS | wValue New address 2 | wIndex 0x0000 | wLength 0 | Time 124.100 us | Time Stamp 4 . 371 101 582
Packet 229318 | SOF 0xA5 | Frame # 1453.7 | CRC5 0x08 | Pkt Len 12 | Time 125.000 us | Time Stamp 4 . 371 225 682
143 Packets 229349-233249 | SOF 0xA5 | Frame # 1454.0 | CRC5 0x0A | Pkt Len 12 | SOF | Time 17.753 ms | Time Stamp 4 . 371 350 682
Transfer 11 | Control GET | ADDR 2 | ENDP 0 | bRequest GET_DESCRIPTOR | wValue DEVICE type | wIndex 0x0000 | Descriptors DEVICE Descriptor | Time 120.618 us | Time Stamp 4 . 389 103 782
Packet 233280 | SOF 0xA5 | Frame # 1471.7 | CRC5 0x12 | Pkt Len 14 | Time 125.000 us | Time Stamp 4 . 389 224 400
S → E
QuickTiming markers not set
Ready
SS ports: Anlz USB3 | Term A:On B:On
Search: Fwd

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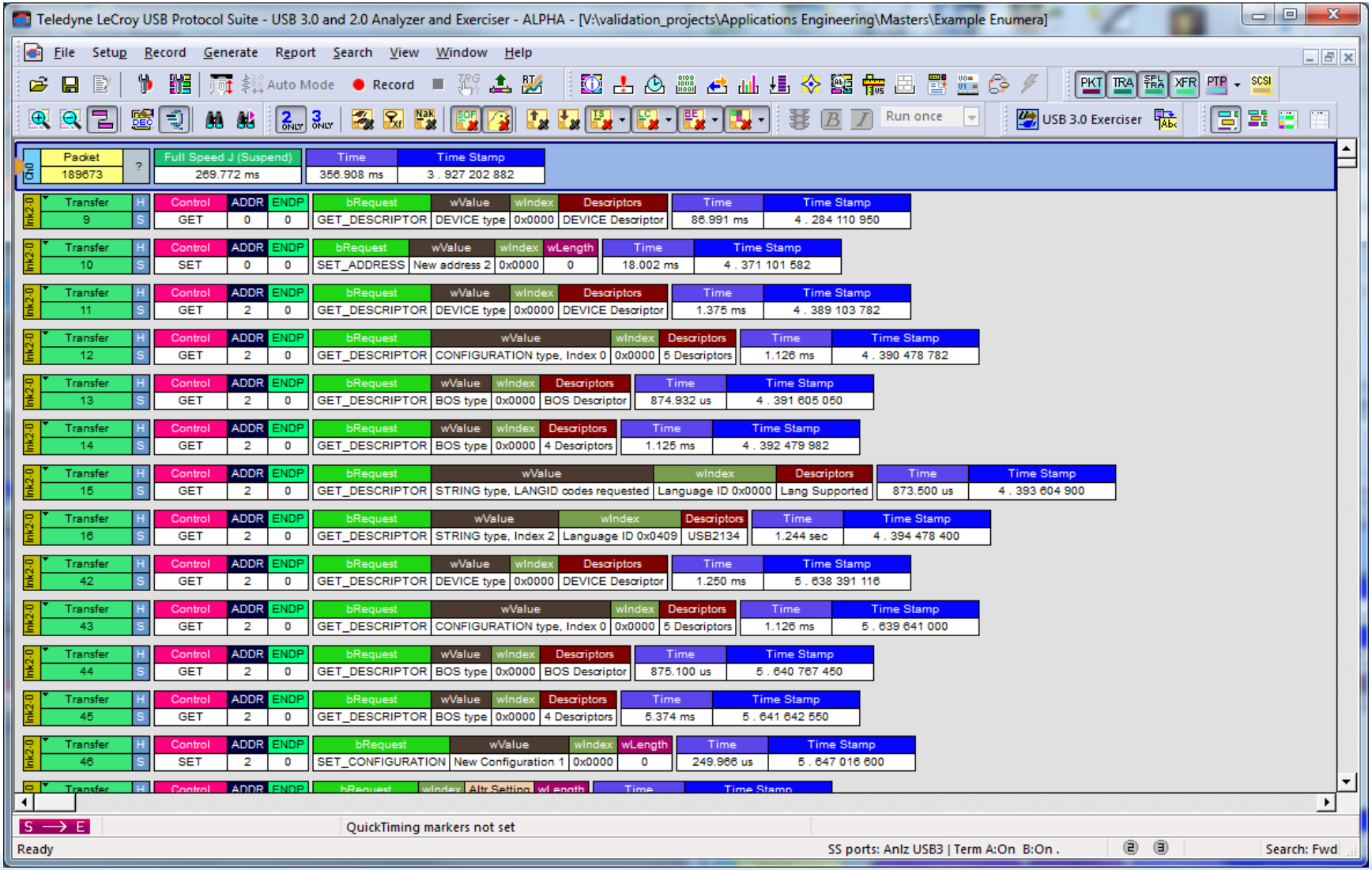
LeCroy Analyzer Screenshots, cont.


Teledyne LeCroy USB Protocol Suite - USB 3.0 and 2.0 Analyzer and Exerciser - ALPHA - [V:\validation_projects\Applications Engineering\Masters\Example Enumera]
File Setup Record Generate Report Search View Window Help
Auto Mode Record Run once USB 3.0 Exerciser
Packet 189673 | Full Speed J (Suspend) 269.772 ms | Time 356.908 ms | Time Stamp 3 . 927 202 882
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Transfer 10 | Control SET | ADDR 0 | ENDP 0 | bRequest SET_ADDRESS | wValue New address 2 | wIndex 0x0000 | wLength 0 | Time 18.002 ms | Time Stamp 4 . 371 101 582
Transfer 11 | Control GET | ADDR 2 | ENDP 0 | bRequest GET_DESCRIPTOR | wValue DEVICE type | wIndex 0x0000 | DEVICE Descriptor | Time 1.375 ms | Time Stamp 4 . 389 103 782
Transfer 12 | Control GET | ADDR 2 | ENDP 0 | bRequest GET_DESCRIPTOR | wValue CONFIGURATION type, Index 0 | wIndex 0x0000 | 5 Descriptors | Time 1.126 ms | Time Stamp 4 . 390 478 782
Transfer 13 | Control GET | ADDR 2 | ENDP 0 | bRequest GET_DESCRIPTOR | wValue BOS type | wIndex 0x0000 | BOS Descriptor | Time 874.932 us | Time Stamp 4 . 391 605 050
Transfer 14 | Control GET | ADDR 2 | ENDP 0 | bRequest GET_DESCRIPTOR | wValue BOS type | wIndex 0x0000 | 4 Descriptors | Time 1.125 ms | Time Stamp 4 . 392 479 982
Transfer 15 | Control GET | ADDR 2 | ENDP 0 | bRequest GET_DESCRIPTOR | wValue STRING type, LANGID codes requested | wIndex Language ID 0x0000 | Descriptors Lang Supported | Time 873.500 us | Time Stamp 4 . 393 604 900
Transfer 16 | Control GET | ADDR 2 | ENDP 0 | bRequest GET_DESCRIPTOR | wValue STRING type, Index 2 | wIndex Language ID 0x0409 | Descriptors USB2134 | Time 1.244 sec | Time Stamp 4 . 394 478 400
Transfer 42 | Control GET | ADDR 2 | ENDP 0 | bRequest GET_DESCRIPTOR | wValue DEVICE type | wIndex 0x0000 | DEVICE Descriptor | Time 1.250 ms | Time Stamp 5 . 638 391 116
Transfer 43 | Control GET | ADDR 2 | ENDP 0 | bRequest GET_DESCRIPTOR | wValue CONFIGURATION type, Index 0 | wIndex 0x0000 | 5 Descriptors | Time 1.126 ms | Time Stamp 5 . 639 641 000
Transfer 44 | Control GET | ADDR 2 | ENDP 0 | bRequest GET_DESCRIPTOR | wValue BOS type | wIndex 0x0000 | BOS Descriptor | Time 875.100 us | Time Stamp 5 . 640 767 450
Transfer 45 | Control GET | ADDR 2 | ENDP 0 | bRequest GET_DESCRIPTOR | wValue BOS type | wIndex 0x0000 | 4 Descriptors | Time 5.374 ms | Time Stamp 5 . 641 642 550
Transfer 46 | Control SET | ADDR 2 | ENDP 0 | bRequest SET_CONFIGURATION | wValue New Configuration 1 | wIndex 0x0000 | wLength 0 | Time 249.966 us | Time Stamp 5 . 647 016 600
QuickTiming markers not set
Ready
SS ports: Anlz USB3 | Term A:On B:On .
Search: Fwd

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USB3.0 HUB

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USB 2.0 to USB 3.0

Backward compatibility with USB 2.0 enables seamless transition

- **Maintain software and device driver infrastructure**
- **Connector compatibility preserves ease-of-use expectation for end user**

End User Perspective		Host (PC, TV, STB, Game Console, etc.)	
		USB 2.0	**USB 3.0**
Device (KB, Mouse, Flash Drive, Printer, Camera, Hard Drive)	**USB 2.0**	Hi-Speed (480Mbps)	Hi-Speed (480Mbps)
	USB 3.0	Hi-Speed (480Mbps)	SuperSpeed (5Gbps)

All Combinations Work!

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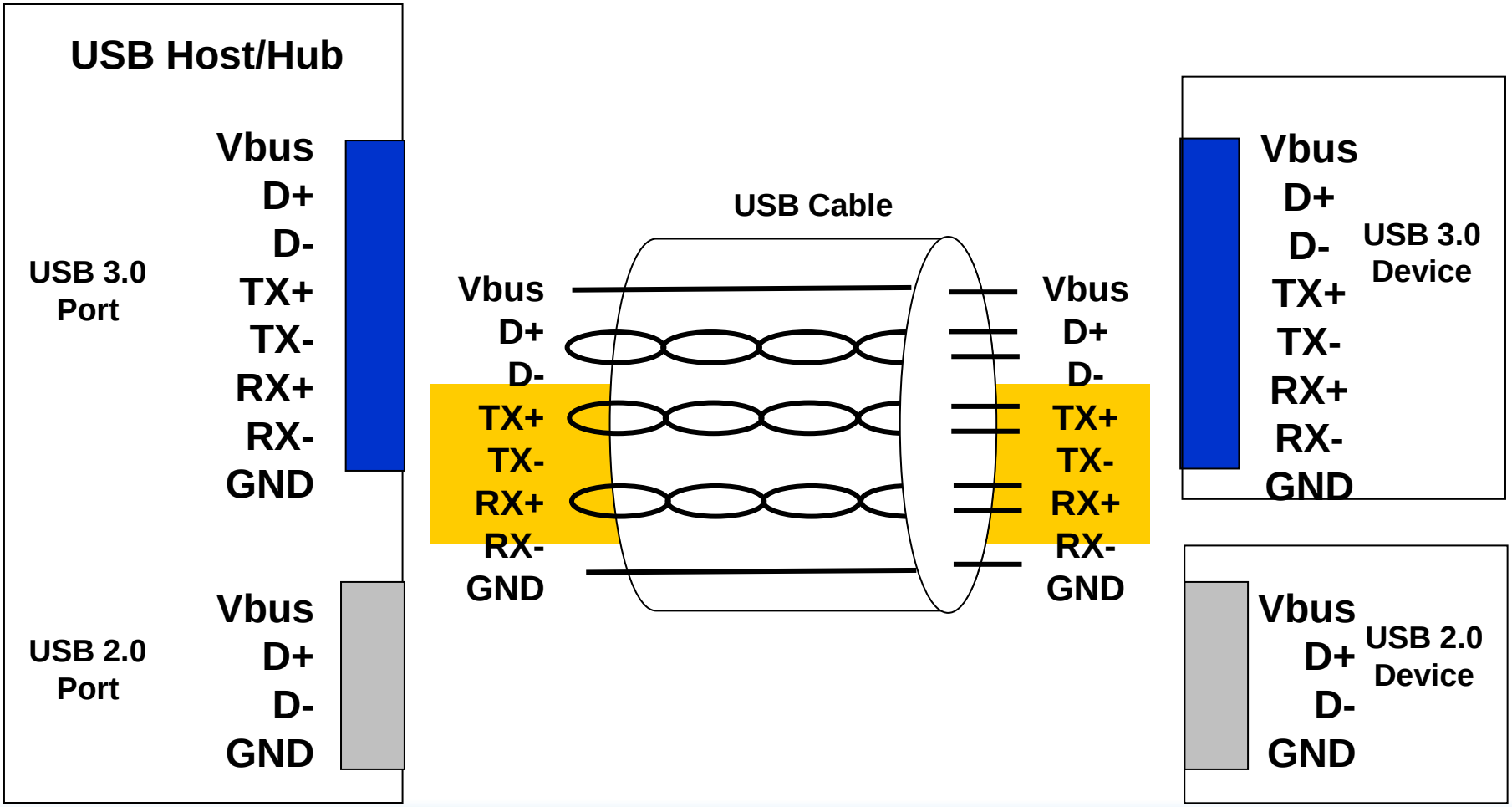
USB 3.0 Topology

- USB 3.0 adds a PCIe-like data pipe and preserves USB 2.0 2-wire interface



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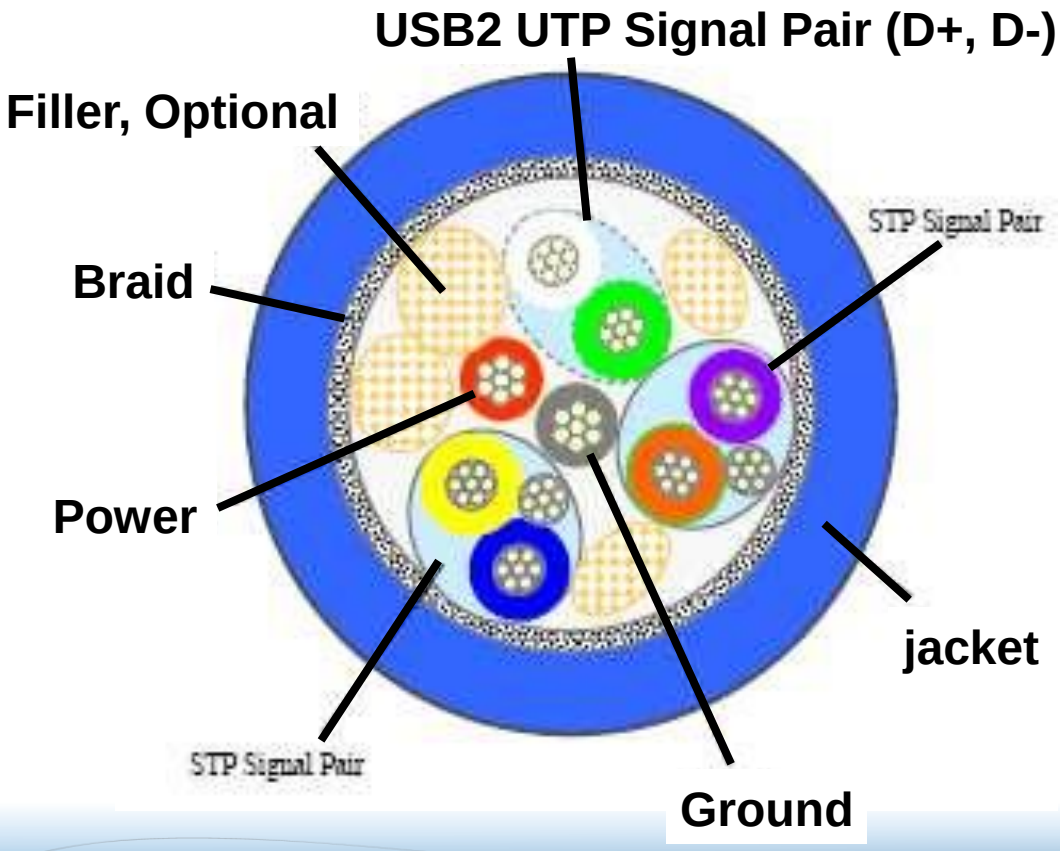
USB 3.0 Cable

- Contains 3 groups of wires – UTP, STP, and power
- Limited to 3 meters in length
- Typical wire gauge is 30-26 AWG



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USB 3.0 Connectors – Std-A

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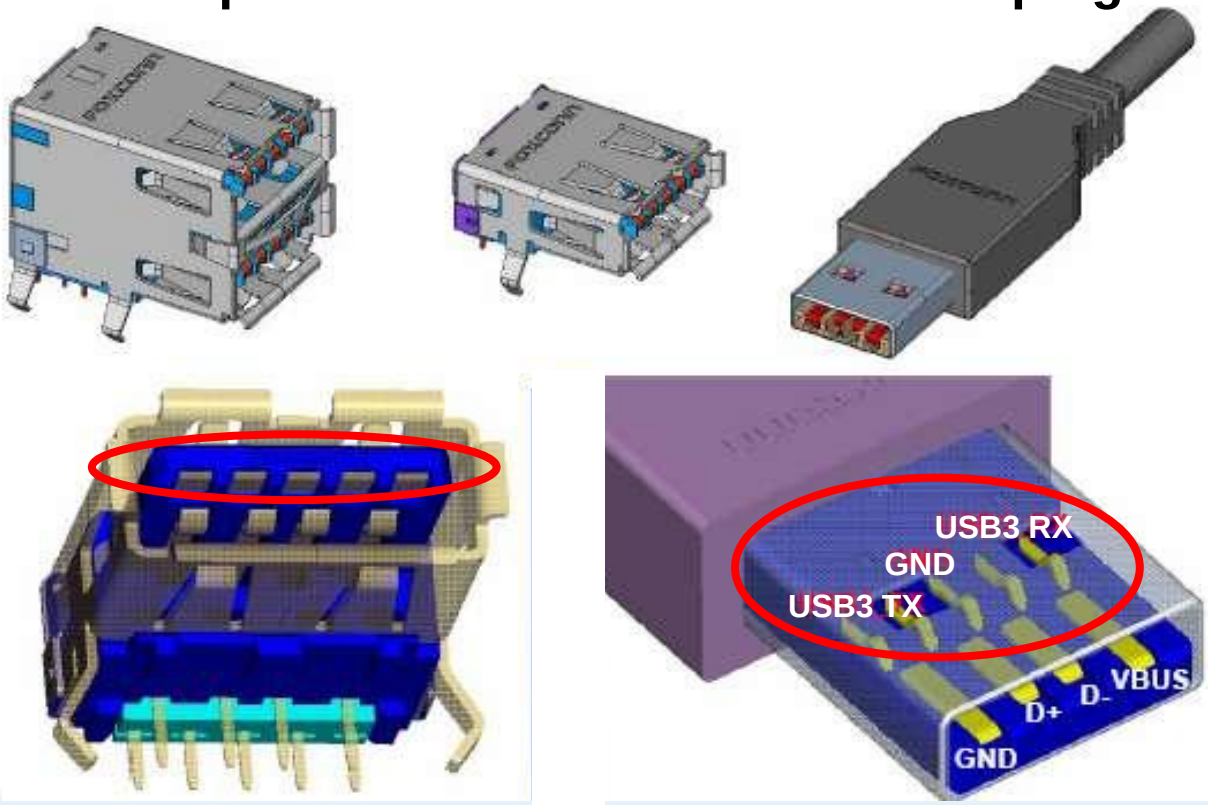
- Std-A connector maintains compatibility with USB 2.0
- Added 2-tier contact pins for USB SuperSpeed
- Blue-color receptacles to uniquely identify USB 3.0-capable ports
- USB 2.0/3.0 Receptacles mates with USB 2.0/3.0 plug



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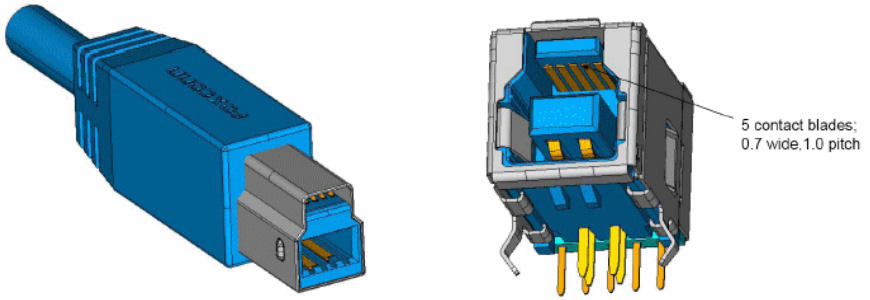
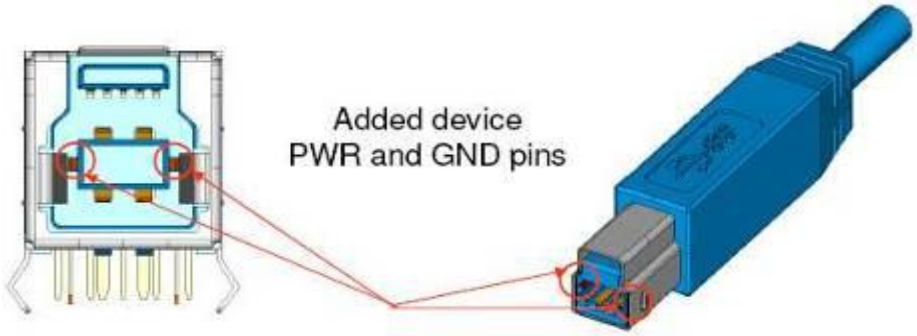
USB 3.0 Connectors – Std-B, Powered-B

- **Standard-B**
  - For large stationary peripherals such as LCD monitor, printers, hard drives, etc.
  - Visually different from USB 2.0 std-B, but the receptacle accepts a USB 2.0 std-B plug



- **Powered-B**
  - Developed for device-powered applications
  - Std-B plus additional Power and ground pins
  - Powered-B receptacle accepts USB 3.0 Powered-B plug, USB 3.0 Std-B plug and USB 2.0 std-B plug



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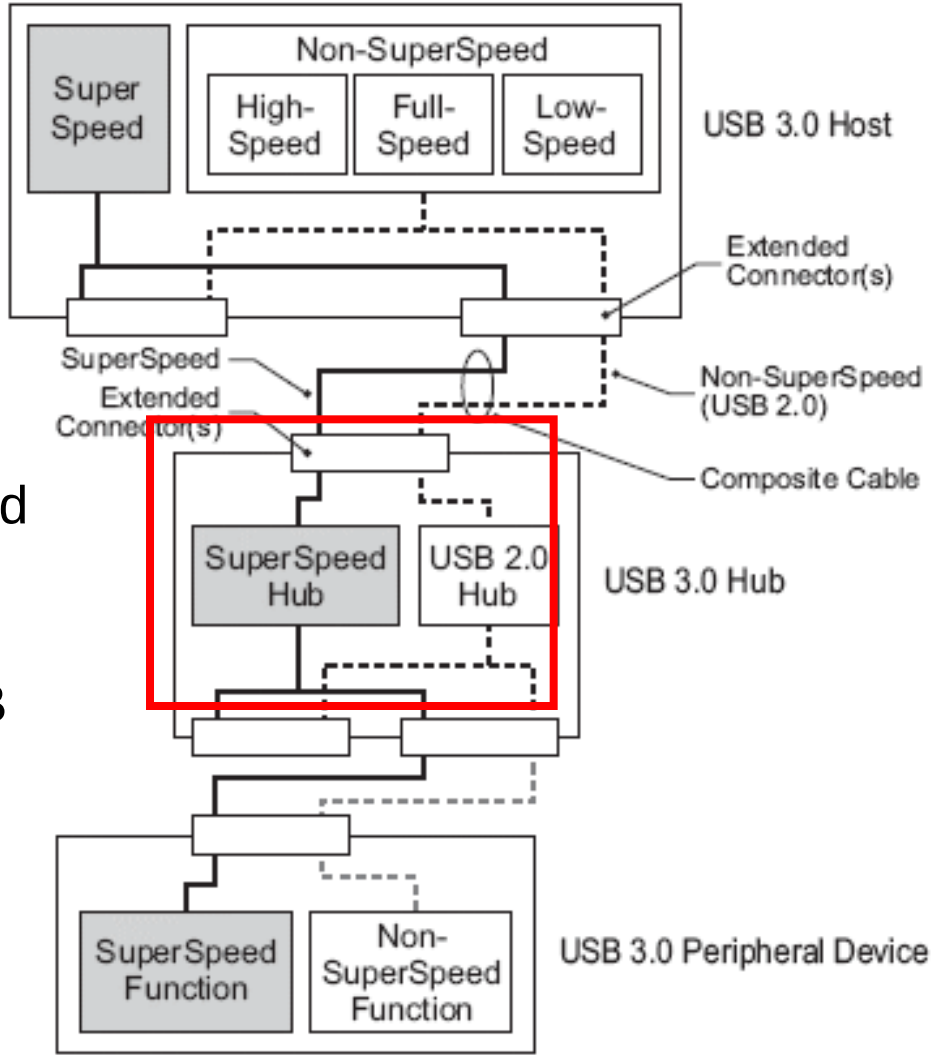
USB 3.0 Hub Architecture

- **Two separate logical controllers**
  - USB 2.0 hub
  - SuperSpeed hub
- **SuperSpeed hub**
  - Not a simple repeater
  - Store and forward headers and data
  - Works like a PCIe switch
  - Connects to host as both USB 2 and SuperSpeed Device
- **Downstream devices**
  - Connect at either USB 2.0 speed or SuperSpeed



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Microchip USB HUB offering

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USB 2.0 Hub Family

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	2-port	3-port	4-port	7-port	SMSC Advantage
Standard Hub *Full-featured USB port expansion solutions*	**USB2422** 36 QFN 4x4	**USB2513B** 36QFN 6x6	**USB2514B** 36 QFN 6x6	**USB2517** 64 QFN 9x9	• High performance, cost effective, market-proven USB2.0 port expansion solutions • MultiTRAK™ - Multiple Transaction Translators (MTT) Architecture • Low power, small footprint • Highly configurable for OEM specific options • Industry-leading USB compatibility • New extended commercial temperature support (USB251xB) • USB Battery Charging spec 1.1 compliant (USB251xB)
USB2 Controller Hub *Next-gen USB2 hubs*	**USB2532** 36 QFN 6x6	**USB2513B** 36 QFN 6x6	**USB2534** 36 QFN 6x6		
Automotive Hub *Automotive-grade (PPAP complete) USB port expansion solutions*			**USB82514** 36/56 QFN 6x6		

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The USB2 Controller HUB

What is a USB Controller Hub

- USB HUB Function (2, 3, 4 port)
- *With* – Embedded Controller
  - GPIO, I²C™, SMbus,
  - Can execute from SPI flash
- *And* End point

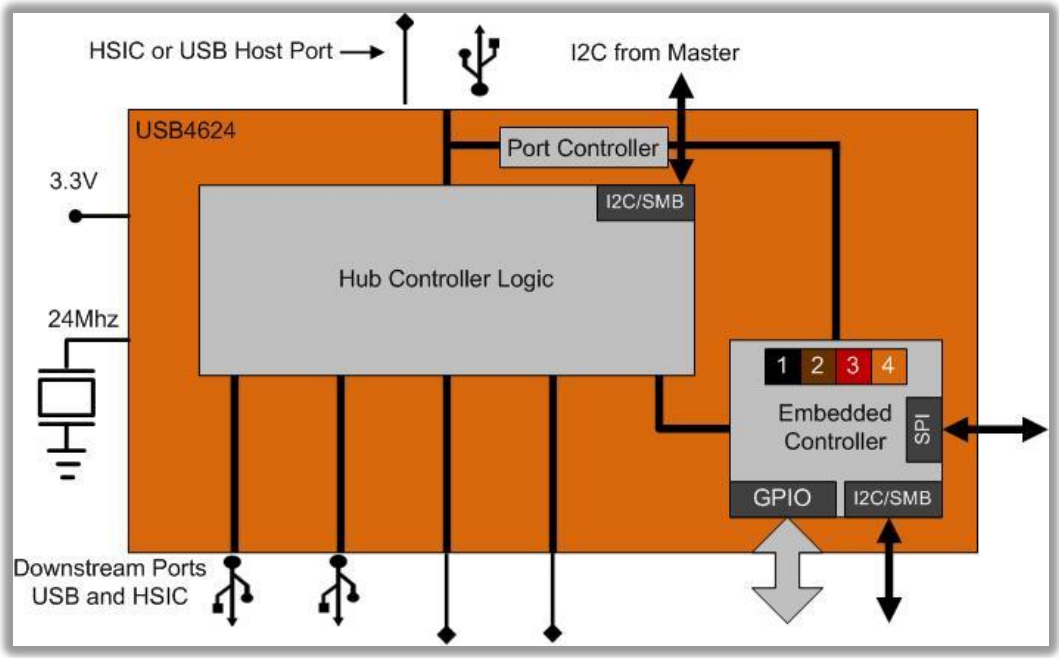
Embedded Controller Functions

- HUB configuration during startup
- "Quad Page" Configuration
- GPIO Bridging for HOST
- Battery Charging Profiles
- Executes custom features

Features Enabled by EC

- Enables HUB GPIO to be directly controlled by HOST system
- Allows independent HUB functions while HOST is powered off
- Allows customer specific functionality into system design

UCH2 = USB2 Controller HUB



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New USB Hub Controller SKUs

USB2 Hub	Upstream	Downstream	Package	Applications
USB2532-1080AEN	USB	USB x2	36 QFN	Hub Controller – 2 Port
USB2533-1080AEN	USB	USB x3	36 QFN	Hub Controller – 3 Port
USB2534-1080AEN	USB	USB x4	36 QFN	Hub Controller – 4 Port
USB4624-1080HN	HSIC/USB	USB x2 / HSIC x2	48 QFN	Hub Controller with USB & HSIC
USB4604-1080HN	HSIC/USB	USB x4	48 QFN	Hub Controller with USB & HSIC
USB3813-1080XY	USB	USB x2 / HSIC x1	30 WLCSP	Mobile Hub Controller
USB3613-1080XY	HSIC	USB x2 / HSIC x1	30 WLCSP	Mobile Low-Power Hub Controller

Naming structure

- USB46YX - HSIC upstream, X - # of ports, Y - # of HSIC ports, 48P QFN
- USB38YX - USB upstream, X - # of ports, Y - # of HSIC ports, 30P WLCSP
- USB36YX - HSIC upstream, X - # of ports, Y - # of HSIC ports, 30P WLCSP
- USB253x- USB upstream, x=number of downstream USB ports, 36P QFN

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USB3.0 HUB options

- USB5537B – Seven Port “Hybrid Hub”
- USB5534B – Four Port Hub
- USB5533B – Three Port Hub
- USB5532B – Two Port Hub

Industry’s Most Complete Hub Product Line

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USB3.0 HUB feature comparison

Features	USB5532B	USB5533B	USB5534B	USB5537B
# of Downstream Ports	2	3	4	7
Package	64QFN	64QFN	64QFN	72QFN
MultiTRAK™	◆	◆	◆	◆
PortMap, PortSwap, TruSpeed, PHYBoost	◆	◆	◆	◆
Vendor Specific Messaging (VSM)	◆	◆	◆	◆
Custom configuration with SPI, SMB	◆	◆	◆	◆
Std Commercial Temp (0 to 70C)	◆	◆	◆	◆
Industrial Temp (-40 to 85C)	◆	◆	◆	◆
BC1.2 & Apple Charging	◆	◆	◆	◆
Support the USC1002 (Advanced Power Management)	◆	◆	◆	◆
Designed for 2-Layer PCBs	◆	◆	◆	◆

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Where to Find More Information

- **USB2.0 and USB3.0 Specifications**
  - http://www.usb.org/developers/docs/
  - Chapter 11 for USB HUB in USB2.0 spec
- **USB Complete book by Jan Axelson**
- **USB Made Simple, a series of articles on USB**
  - http://www.usbmadesimple.co.uk/
- **Microchip USB HUBs Data Sheets and Application Notes**
  - http://www.smsc.com/Products/USB/USB_Hubs

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Summary

- USB2.0 and USB3.0 have become most ubiquitous interfaces in commercial and embedded applications
- USB HUB is one of the most important elements in the USB topology
- Power consumption is very critical when designing with HUBs
- Signals integrity and protocol compliance are key factors, especially to obtain the USB Logos
- Microchip has the largest and most features rich family of USB HUBs

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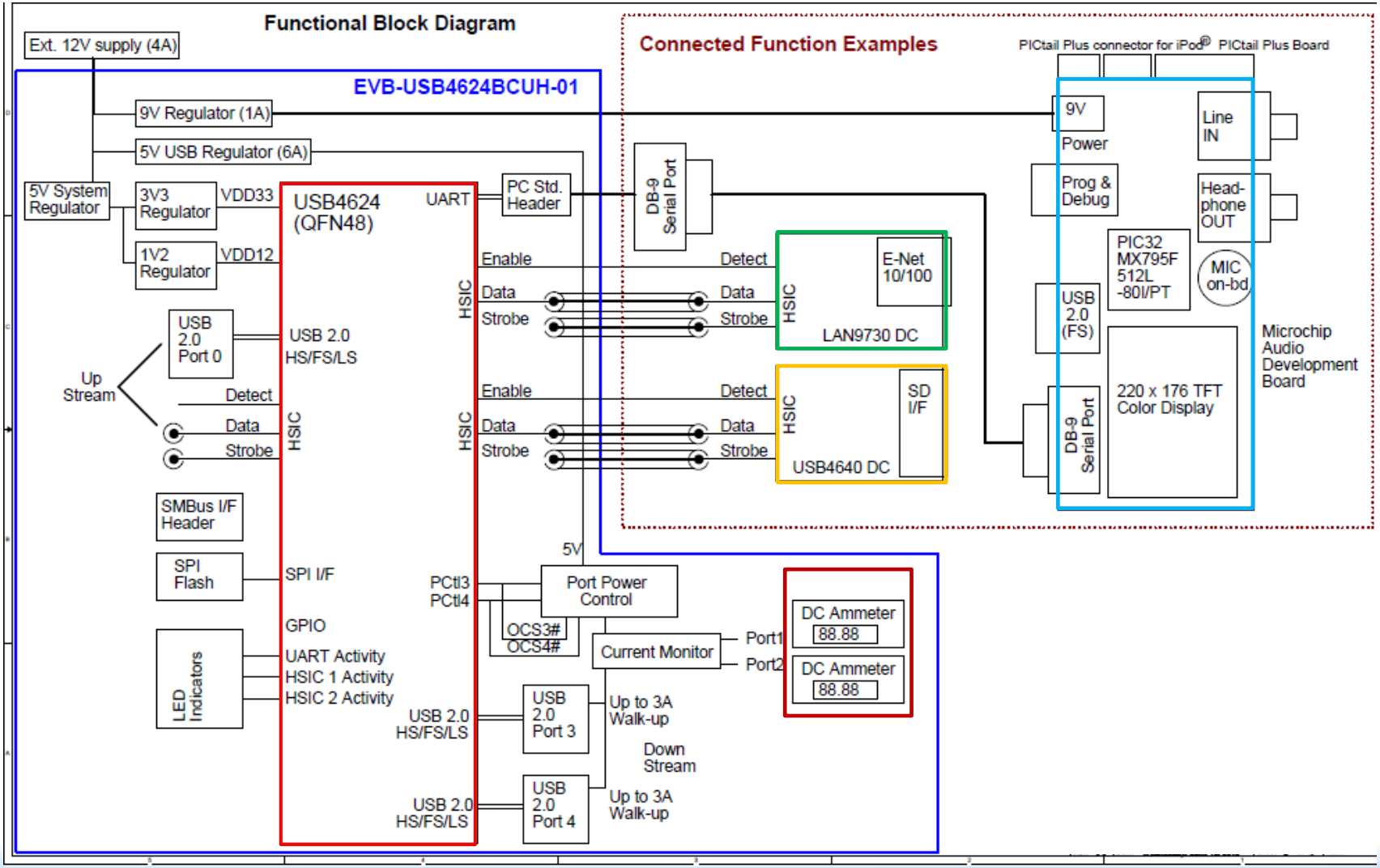
Demo board diagram



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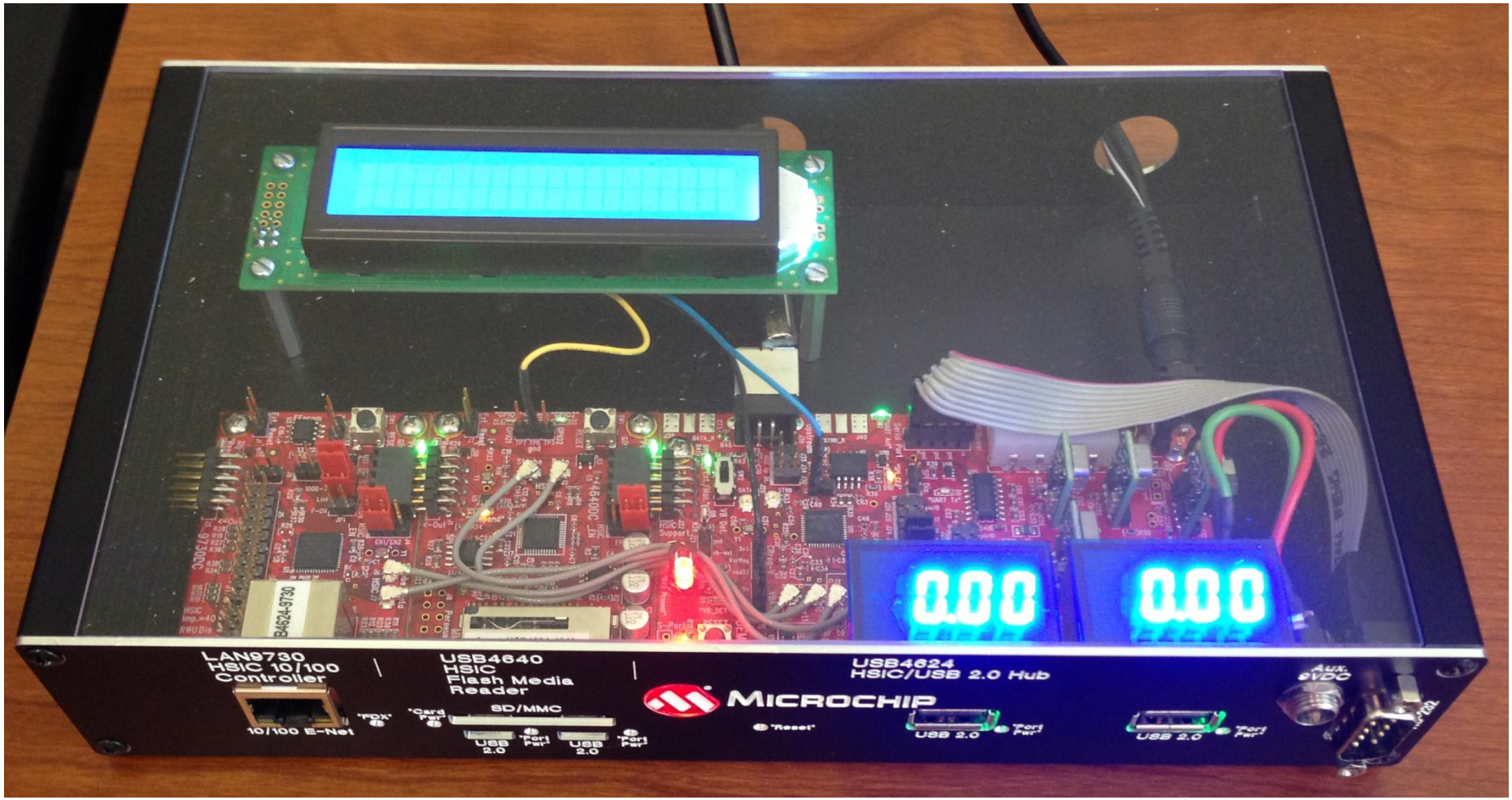
Demo

USB46XX Demo



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